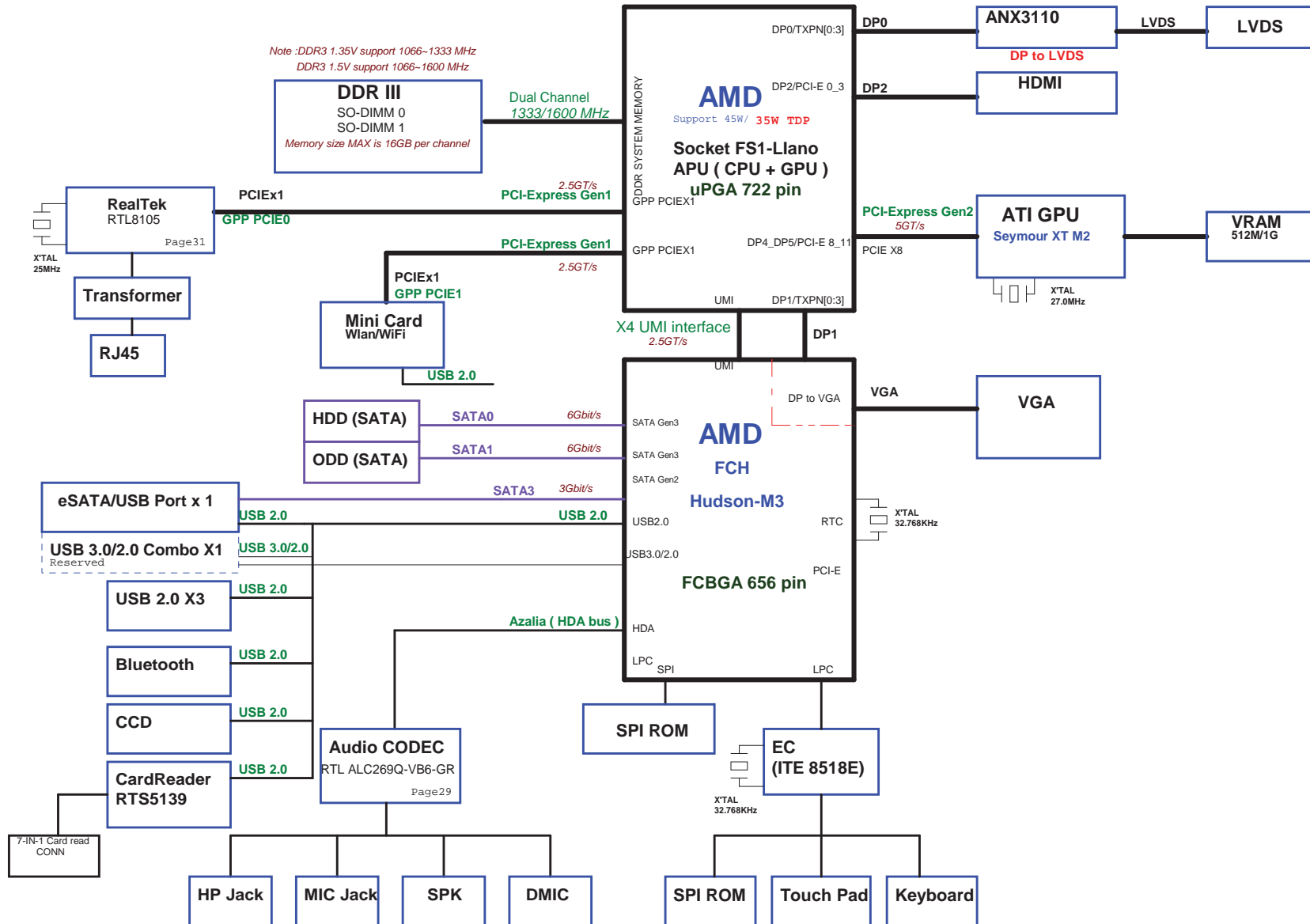


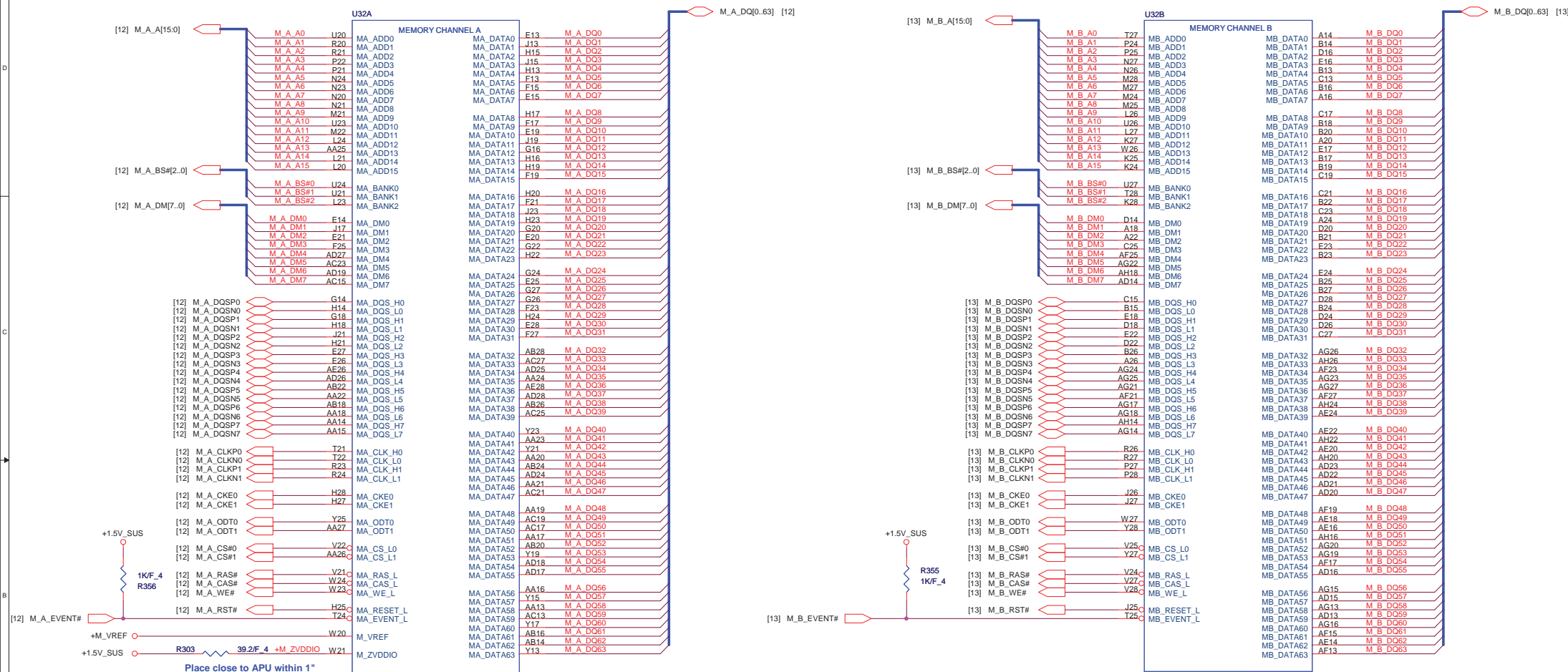
## BLOCK DIAGRAM

Note :DP means Display Port Interface



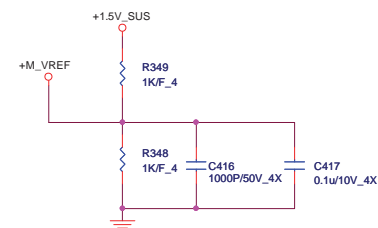
Discharge	Page37
Charge	Page38
DDR3/0.75V (RT8207)	Page39
3V/5V (RT8205)	Page40
1.1V/+1.0V_GPU	Page41
+1.2V_VDDPR/+2.5	Page42
VDD/+VDDNB_CORE	Page43
GFX_CORE (OZ8117)	Page44
+1.8V_GPU (HFA00835RTER)	Page45



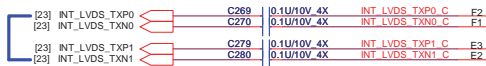


## Liano APU

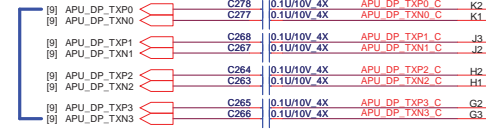
## Liano APU



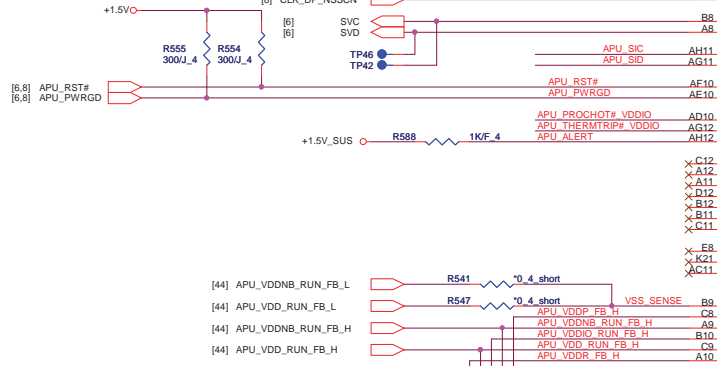
DP0 to LVDS



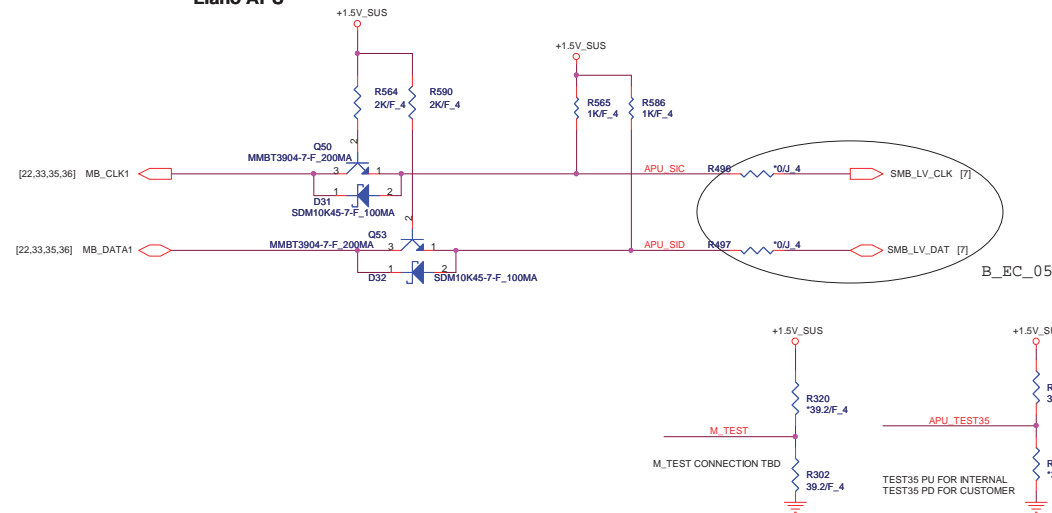
DP1 to Hudson-M3 VGA output



Note: CLK\_APU\_HCLKP/N is 100MHz SSC



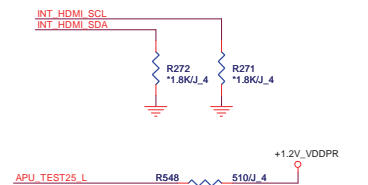
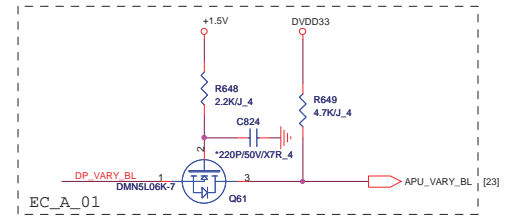
Llano APU



LVDS

VGA

HDMI



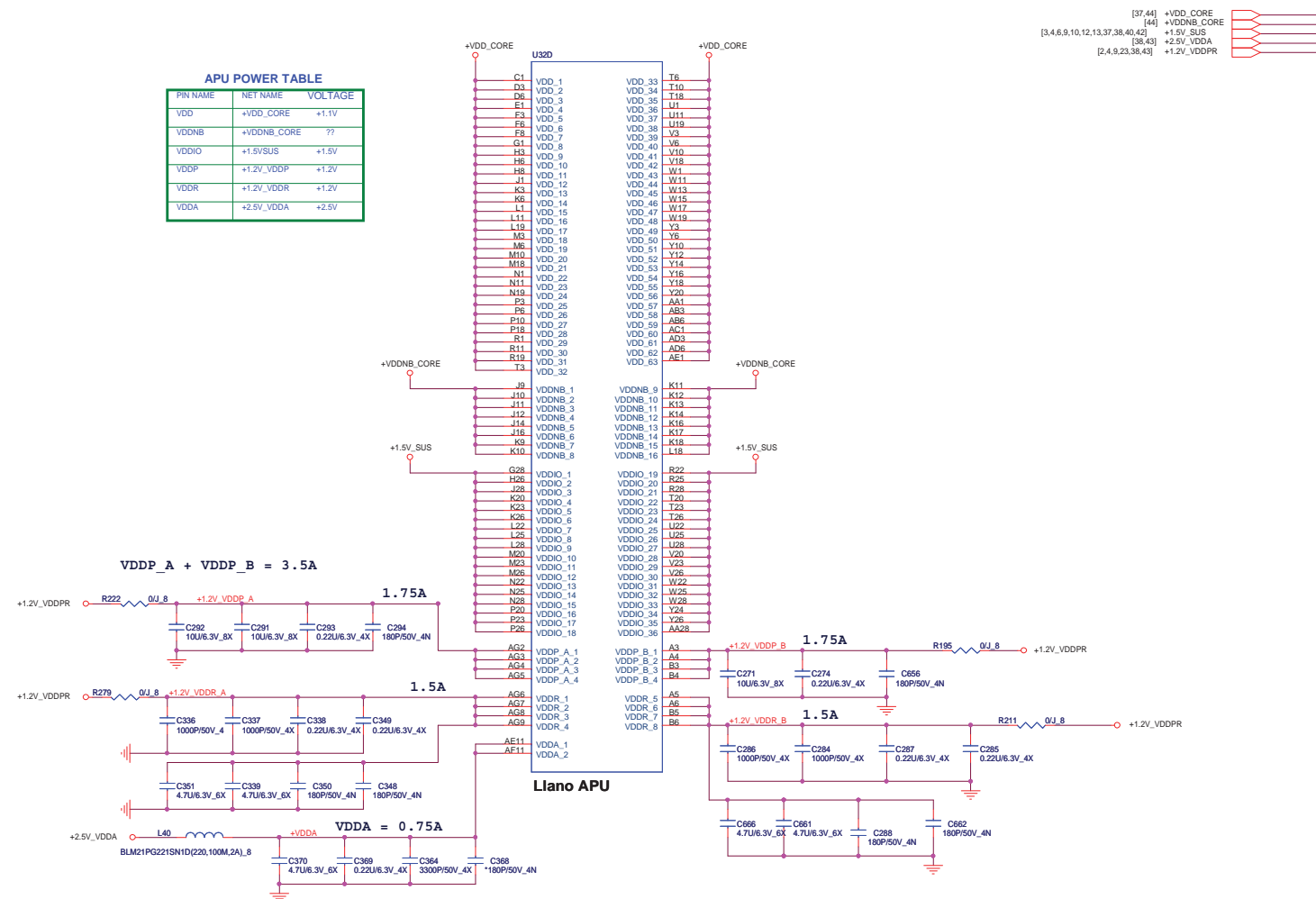
**PROJECT : KL6B/C**  
**Quanta Computer Inc.**

Size Document Number  
**Llano Display/Misc**

Date: Thursday, April 28, 2011 Sheet 4 of 49 Rev 1A

APU POWER TABLE

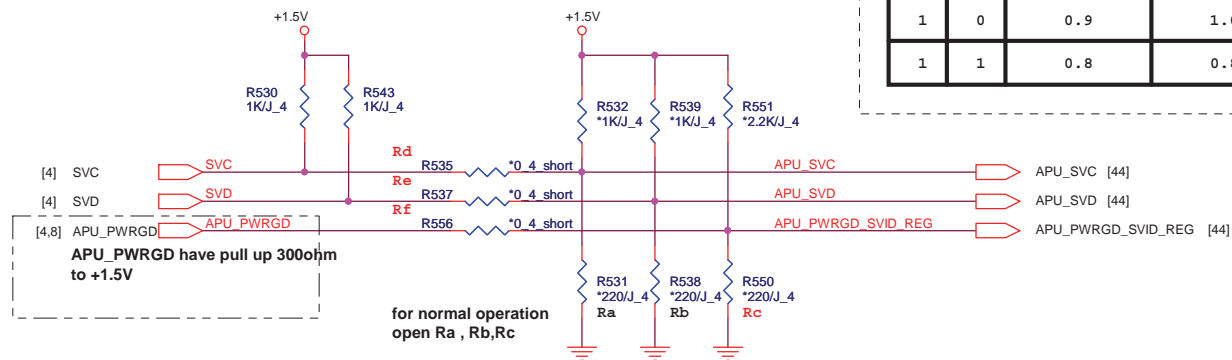
PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



U32E		
AZ	VSS_1	VSS_75
A13	VSS_2	T11
A15	VSS_3	T19
A17	VSS_4	U4
A19	VSS_5	U7
A21	VSS_6	U10
A23	VSS_7	U18
A25	VSS_8	V9
B7	VSS_9	V11
B8	VSS_10	V19
B9	VSS_11	W4
C4	VSS_12	W7
C10	VSS_13	W10
C11	VSS_14	W12
C14	VSS_15	W14
C16	VSS_16	W16
C18	VSS_17	W18
C20	VSS_18	Y9
C22	VSS_19	Y22
C24	VSS_20	Y24
C26	VSS_21	Y26
C28	VSS_22	Y28
C30	VSS_23	Y30
C32	VSS_24	Y32
C34	VSS_25	Y34
C36	VSS_26	Y36
C38	VSS_27	Y38
C40	VSS_28	Y40
C42	VSS_29	Y42
C44	VSS_30	Y44
C46	VSS_31	Y46
C48	VSS_32	Y48
C50	VSS_33	Y50
C52	VSS_34	Y52
C54	VSS_35	Y54
C56	VSS_36	Y56
C58	VSS_37	Y58
C60	VSS_38	Y60
C62	VSS_39	Y62
C64	VSS_40	Y64
C66	VSS_41	Y66
C68	VSS_42	Y68
C70	VSS_43	Y70
C72	VSS_44	Y72
C74	VSS_45	Y74
C76	VSS_46	Y76
C78	VSS_47	Y78
C80	VSS_48	Y80
C82	VSS_49	Y82
C84	VSS_50	Y84
C86	VSS_51	Y86
C88	VSS_52	Y88
C90	VSS_53	Y90
C92	VSS_54	Y92
C94	VSS_55	Y94
C96	VSS_56	Y96
C98	VSS_57	Y98
C100	VSS_58	Y100
C102	VSS_59	Y102
C104	VSS_60	Y104
C106	VSS_61	Y106
C108	VSS_62	Y108
C110	VSS_63	Y110
C112	VSS_64	Y112
C114	VSS_65	Y114
C116	VSS_66	Y116
C118	VSS_67	Y118
C120	VSS_68	Y120
C122	VSS_69	Y122
C124	VSS_70	Y124
C126	VSS_71	Y126
C128	VSS_72	Y128
C130	VSS_73	Y130
C132	VSS_74	Y132
C134	VSS_75	Y134
C136	VSS_76	Y136
C138	VSS_77	Y138
C140	VSS_78	Y140
C142	VSS_79	Y142
C144	VSS_80	Y144
C146	VSS_81	Y146
C148	VSS_82	Y148
C150	VSS_83	Y150
C152	VSS_84	Y152
C154	VSS_85	Y154
C156	VSS_86	Y156
C158	VSS_87	Y158
C160	VSS_88	Y160
C162	VSS_89	Y162
C164	VSS_90	Y164
C166	VSS_91	Y166
C168	VSS_92	Y168
C170	VSS_93	Y170
C172	VSS_94	Y172
C174	VSS_95	Y174
C176	VSS_96	Y176
C178	VSS_97	Y178
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C194	VSS_105	Y194
C196	VSS_106	Y196
C198	VSS_107	Y198
C200	VSS_108	Y200
C202	VSS_109	Y202
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C206	VSS_111	Y206
C208	VSS_112	Y208
C210	VSS_113	Y210
C212	VSS_114	Y212
C214	VSS_115	Y214
C216	VSS_116	Y216
C218	VSS_117	Y218
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C224	VSS_120	Y224
C226	VSS_121	Y226
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C246	VSS_131	Y246
C248	VSS_132	Y248
C250	VSS_133	Y250
C252	VSS_134	Y252
C254	VSS_135	Y254
C256	VSS_136	Y256
C258	VSS_137	Y258
C260	VSS_138	Y260
C262	VSS_139	Y262
C264	VSS_140	Y264
C266	VSS_141	Y266
C268	VSS_142	Y268
C270	VSS_143	Y270
C272	VSS_144	Y272
C274	VSS_145	Y274
C276	VSS_146	Y276
C278	VSS_147	Y278
C280	VSS_148	Y280
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C288	VSS_152	Y288
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C292	VSS_154	Y292
C294	VSS_155	Y294
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C306	VSS_161	Y306
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C312	VSS_164	Y312
C314	VSS_165	Y314
C316	VSS_166	Y316
C318	VSS_167	Y318
C320	VSS_168	Y320
C322	VSS_169	Y322
C324	VSS_170	Y324
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C354	VSS_185	Y354
C356	VSS_186	Y356
C358	VSS_187	Y358
C360	VSS_188	Y360
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C414	VSS_215	Y414
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C418	VSS_217	Y418
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C424	VSS_220	Y424
C426	VSS_221	Y426
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C434	VSS_225	Y434
C436	VSS_226	Y436
C438	VSS_227	Y438
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C474	VSS_245	Y474
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C620	VSS_318	Y620
C622	VSS_319	Y622
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C626	VSS_321	Y626
C628	VSS_322	Y628
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C716	VSS_366	Y716
C718	VSS_367	Y718
C720	VSS_368	Y720
C722	VSS_369	Y722
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C726	VSS_371	Y726
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C748	VSS_382	Y748
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C756	VSS_386	Y756
C758	VSS_387	Y758
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C762	VSS_389	Y762
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C766	VSS_391	Y766
C768	VSS_392	Y768
C770	VSS_393	Y770
C772	VSS_394	Y772
C774	VSS_395	Y774
C776	VSS_396	Y776
C778	VSS_397	Y778
C780	VSS_398	Y780
C782	VSS_399	Y782
C784	VSS_400	Y784
C786	VSS_401	Y786
C788	VSS_402	Y788
C790	VSS_403	Y790
C792	VSS_404	Y792
C794	VSS_405	Y794
C796	VSS_406	Y796
C798	VSS_407	

## VID Override Circuit

**Note:**  
To override VID, Remove Rd, Re, Rf, install Rc  
set VID via SVC & SVD option RES.



## BOOT VOLTAGE

SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

[4,8,9,23,25,28,29,42] +1.5V  
[3,4,5,9,10,12,13,37,38,40,42] +1.5V\_SUS

06

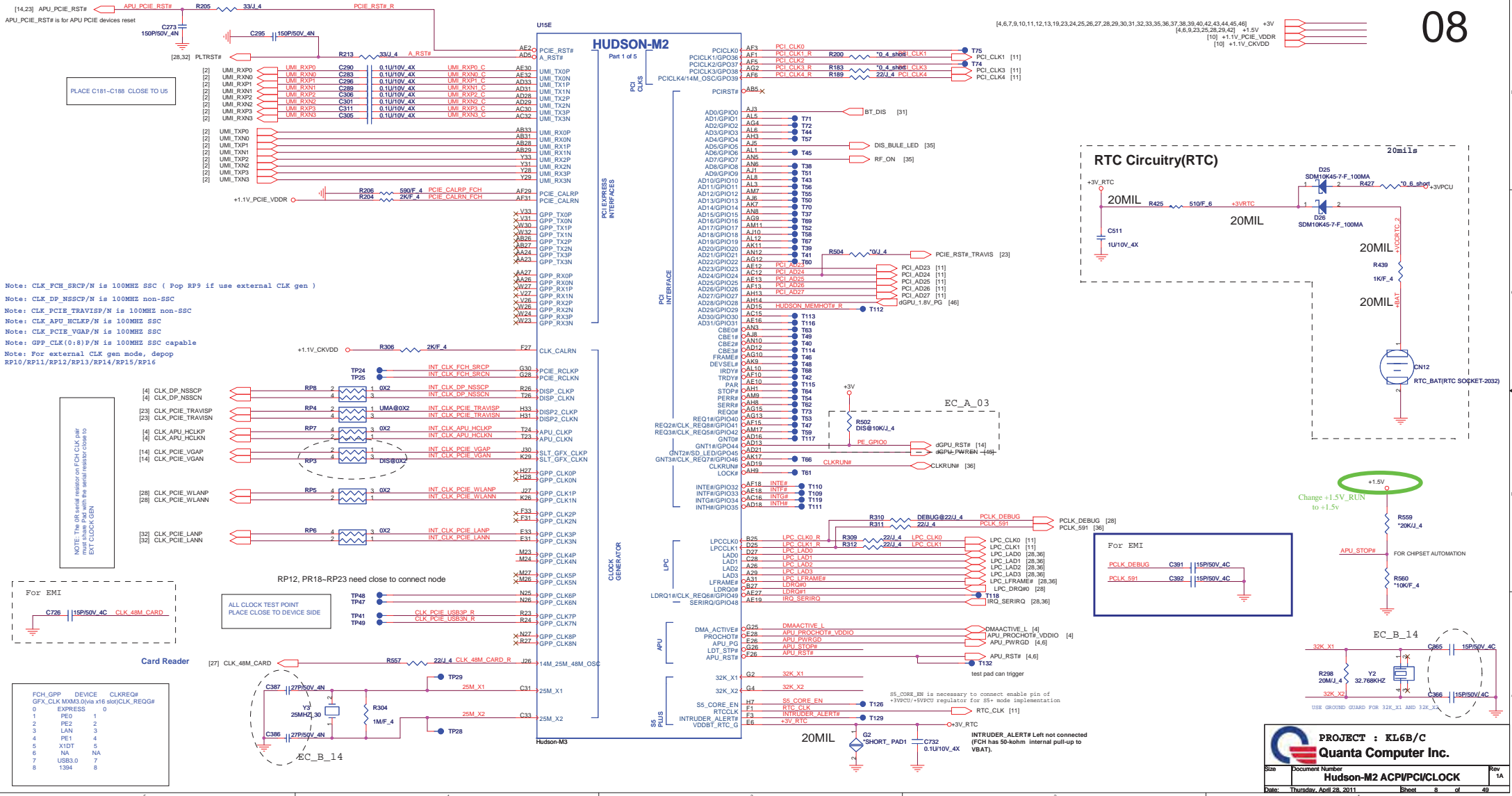
## HDT+ Connector

Debug only

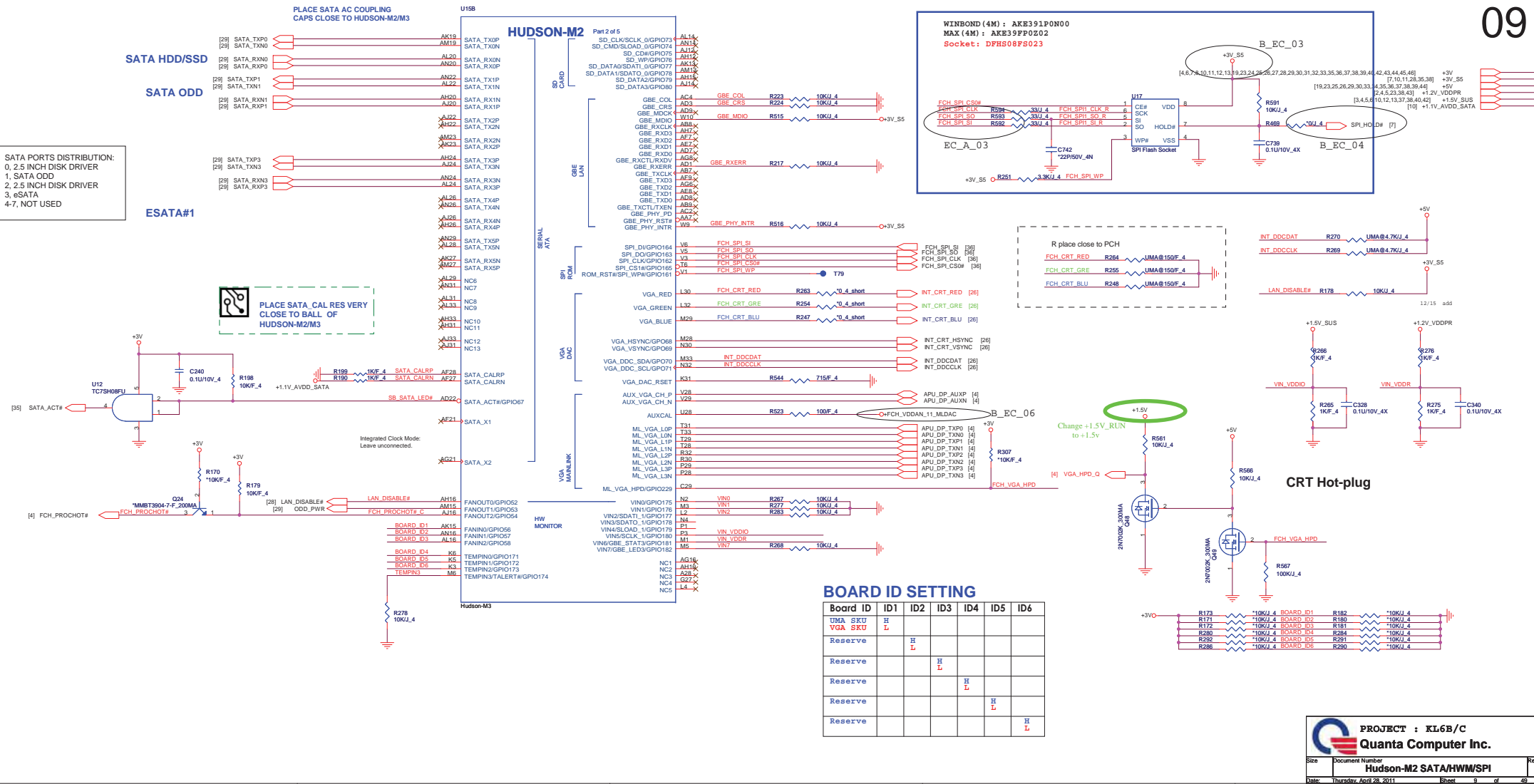
 <b>PROJECT : KL6B/C</b> <b>Quanta Computer Inc.</b>		Rev 1A
Size	Document Number	
<b>Llano DEBUG&amp;OTHER</b>		
Date:	Thursday, April 28, 2011	Sheet 6 of 49









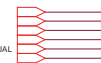


**PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.**

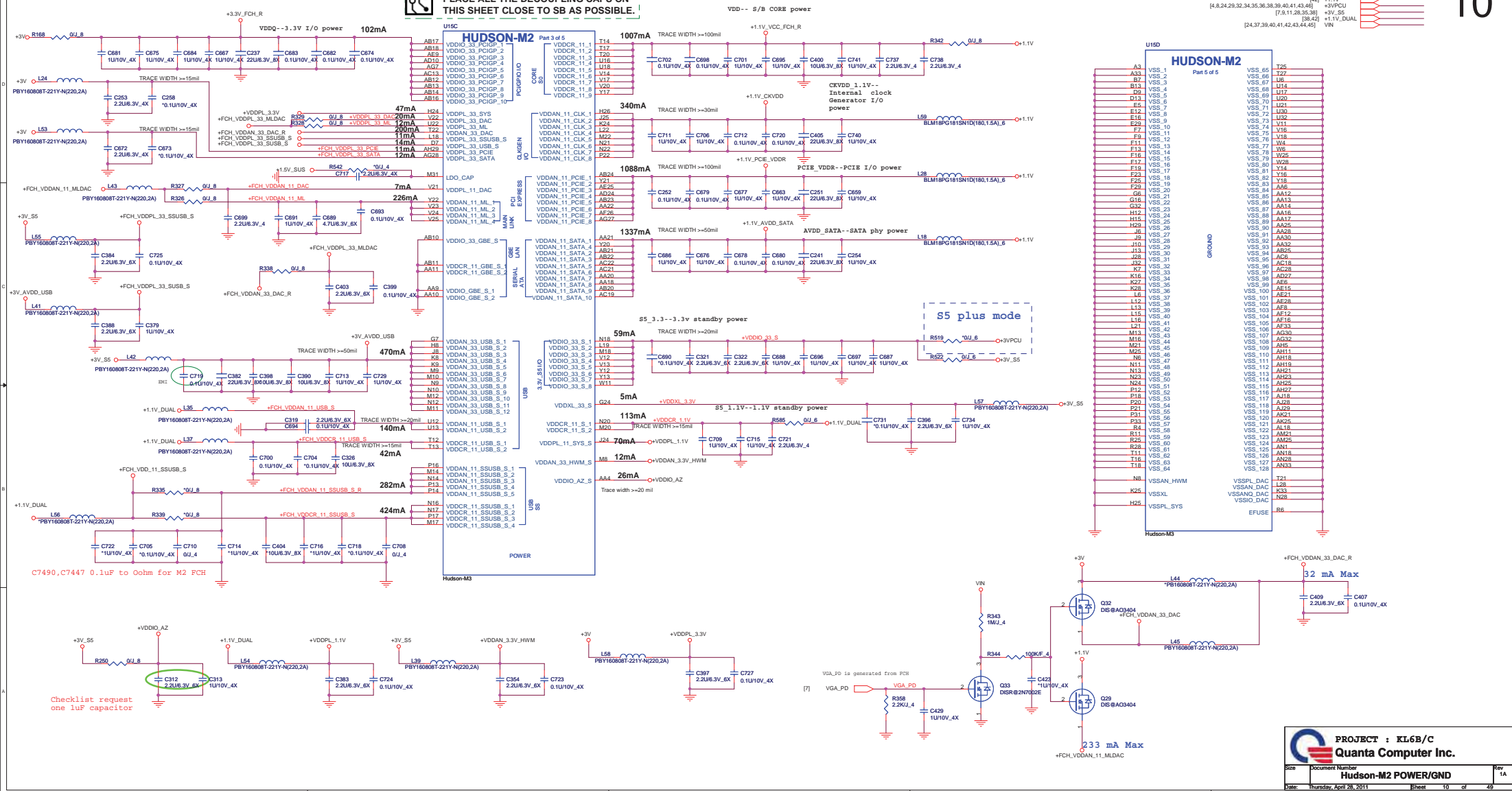
VDD-- S/B CORE power

[4,6,7,8,9,11,12,13,19,23,24,25,26,27,28,29,30,31,32,33,35,36,37,38,39,40,42,43,44,45,46]  
[4,8,24,29,32,34,35,36,38,39,40,41,43,46]  
[7,9,11,28,35,38]  
[38,41]  
[24,37,39,40,41,42,43,44,45]

	+3V
[42]	+1.1V
[46]	+3V
[5,38]	+3V
[38,42]	+1.1V
[4,45]	VIN



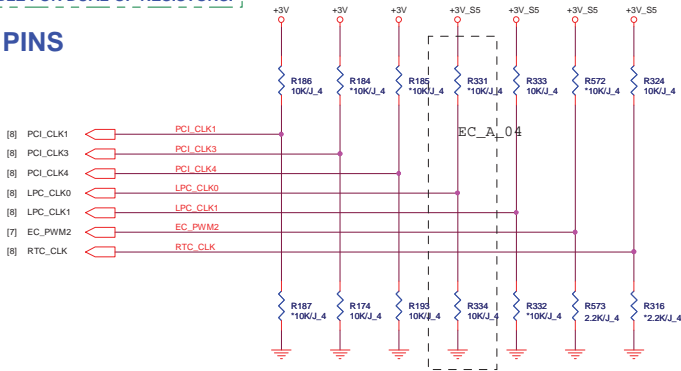
10





OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

## STRAPS PINS

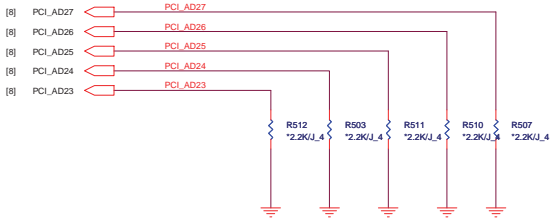


### REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

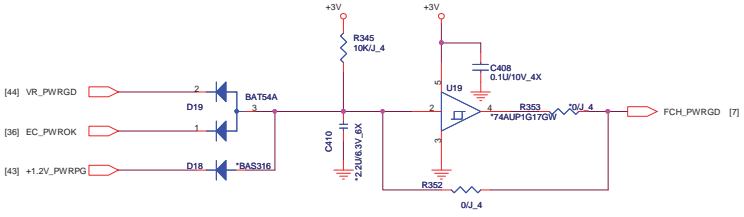
## DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

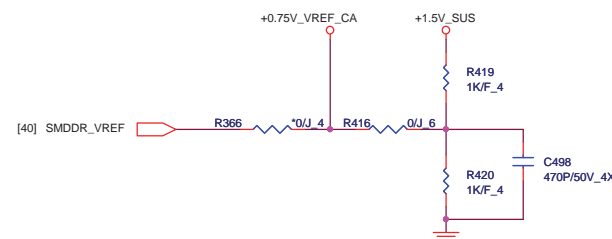


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

[4,6,7,8,9,10,12,13,19,23,24,25,26,27,28,29,30,31,32,33,35,36,37,38,39,40,42,43,44,45,46] +3V [7,8,10,28,35,38] +3V\_S5

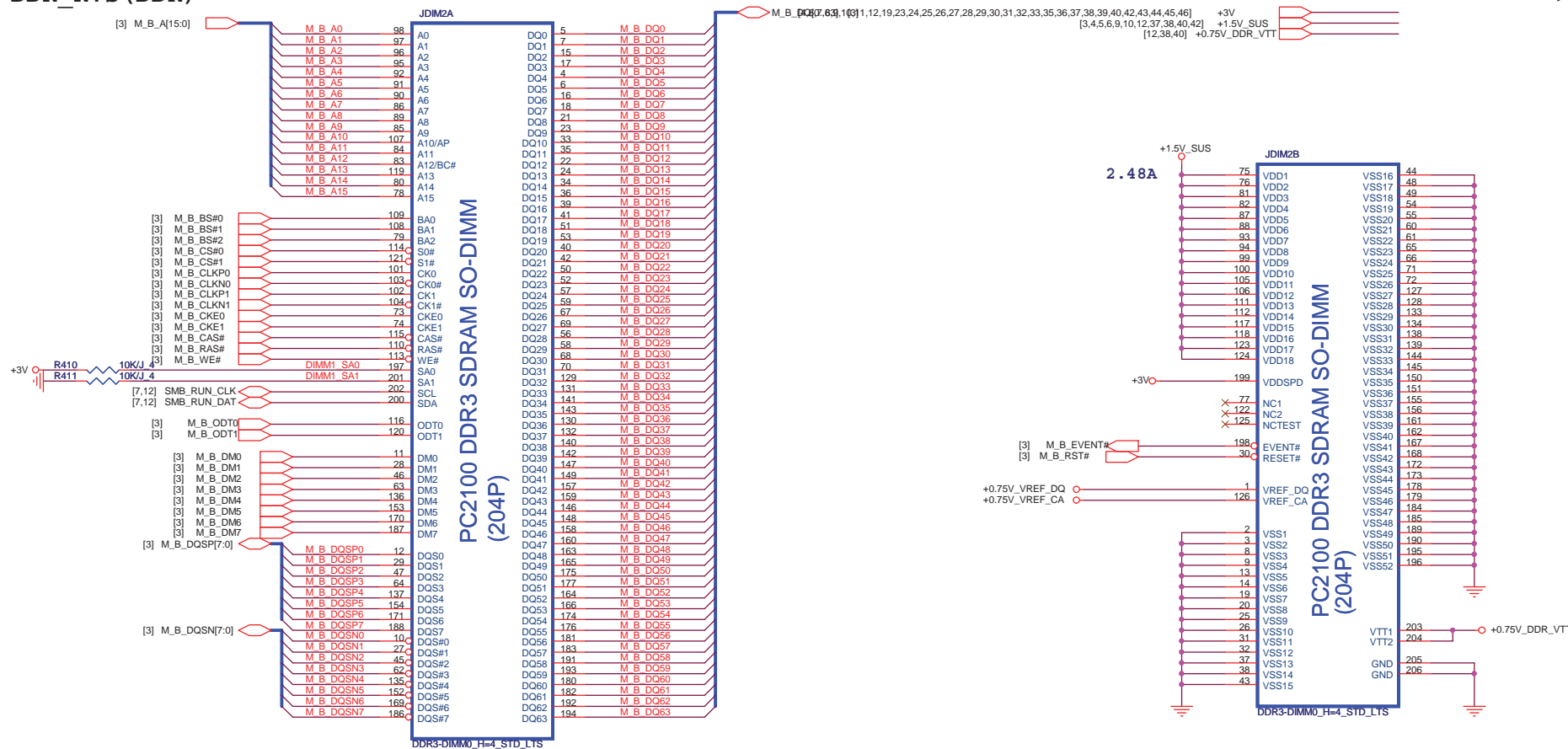


FCH PWRGD CKT

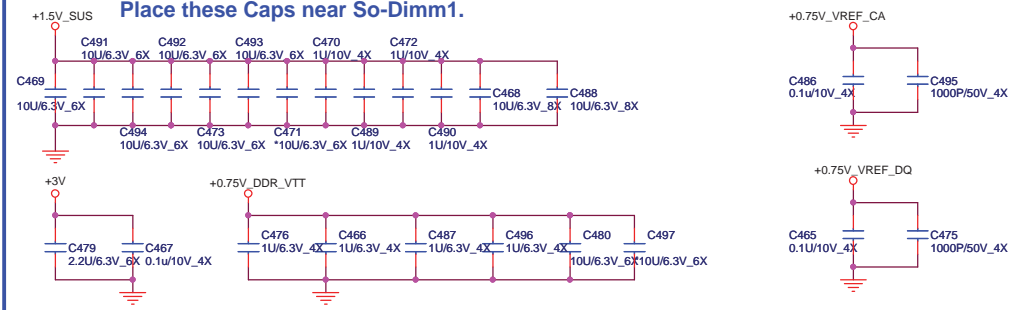


# DDR\_RVS (DDR)

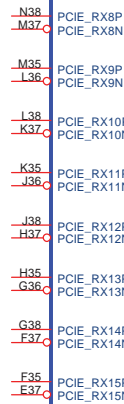
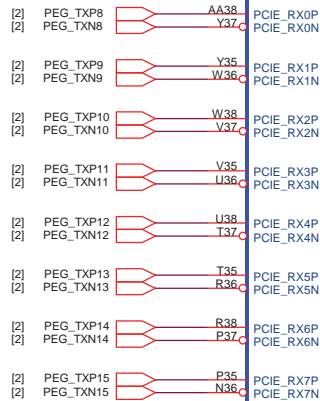
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## Place these Caps near So-Dimm1.



5GT/s bit rate



[8] CLK\_PCIE\_VGAP  
[8] CLK\_PCIE\_VGAN

For M97 only Madison and Park the PWRGOOD ball is for test purposes and must be connected to ground



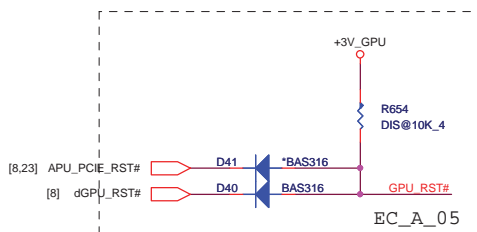
DIS@Seymour\_M2

PCI EXPRESS INTERFACE

CALIBRATION



[15,17,18,38,40] +1V\_GPU

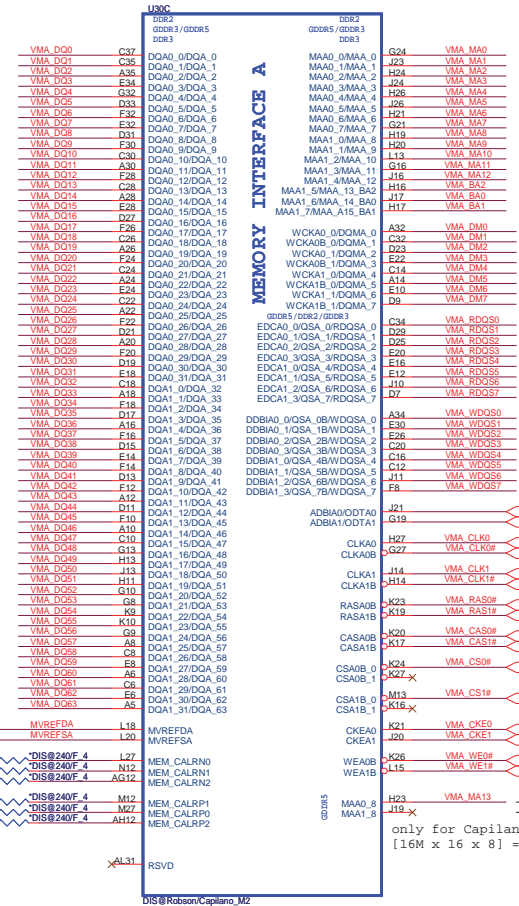
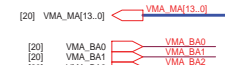






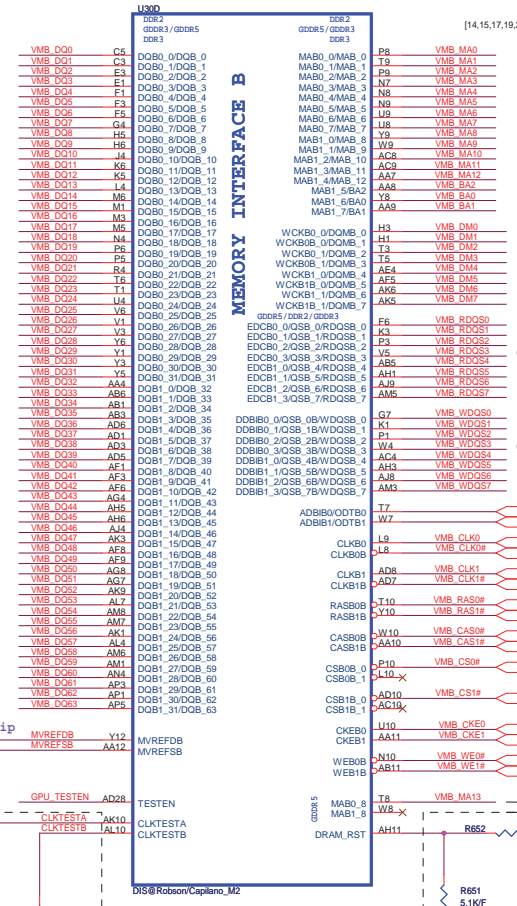
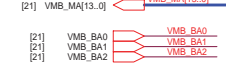
# Seymour M2 use Memory Group B only

16

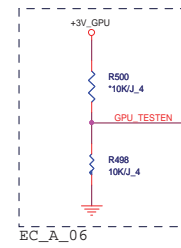


Ball Name	Seymour M2	Capilano M2
MVREFDA	NC	V
MVREFSA	NC	V
MVREFDB	V	V
MVREFSB	V	V
MEM_CALRN0	NC	V
MEM_CALRN1	V	V
MEM_CALRN2	NC	V
MEM_CALRP0	NC	V
MEM_CALRP1	V	V
MEM_CALRP2	NC	V

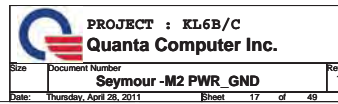
DDR3/GDDR3 Memory Stuff Option	
Robson/Capilano	DDR3
MVDDQ	1.5V
Ra	40.2R
Rb	100R



TESTEN	Description
0	Internal Debug use only
1	JTAG signals enable



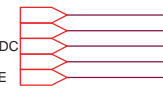
## 17



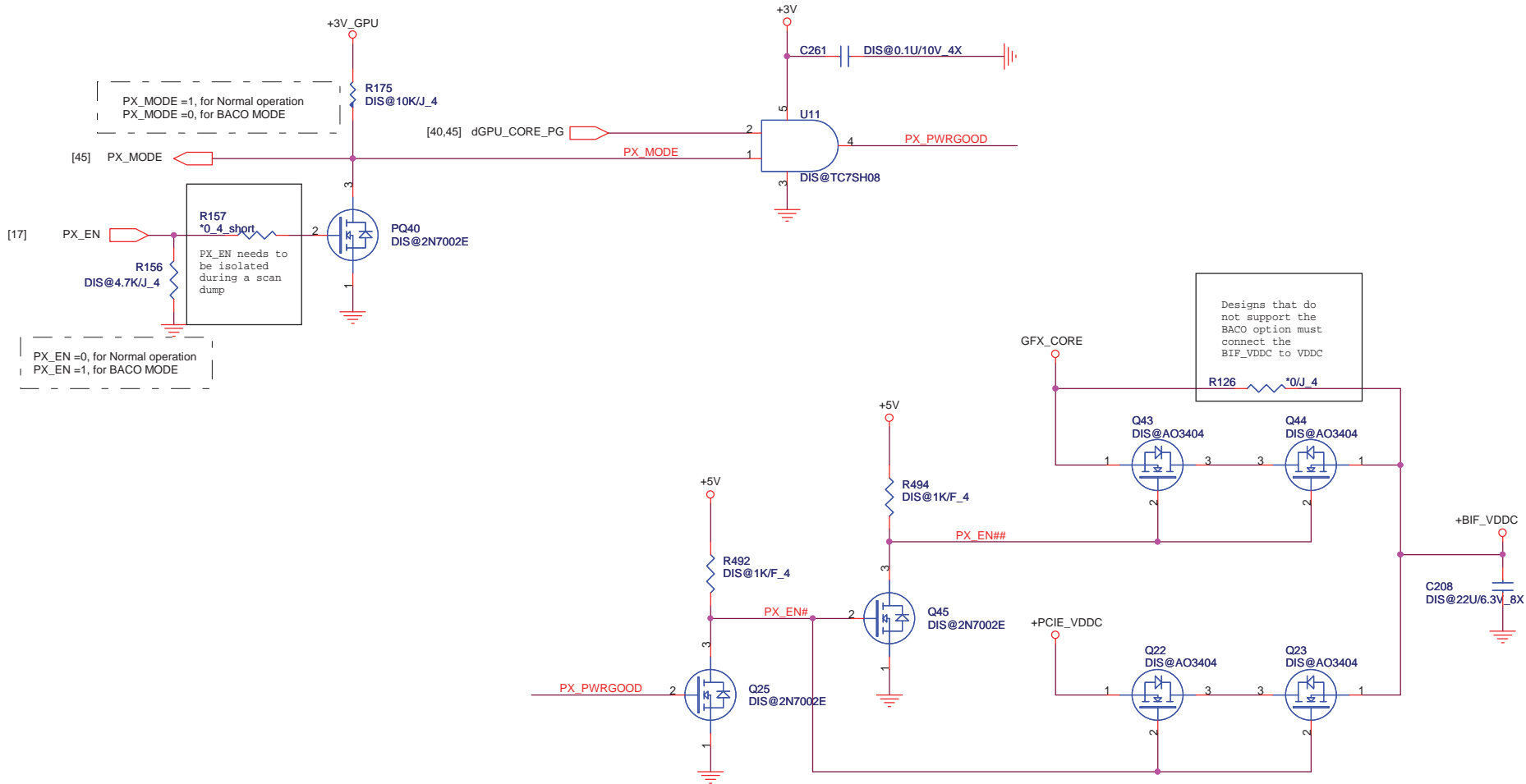


[4,6,7,8,9,10,11,12,13,23,24,25,26,27,28,29,30,31,32,33,35,36,37,38,39,40,42,43,44,45,46]  
 [9,23,25,26,29,30,33,34,35,36,37,38,39,44]  
 [14,15,16,17,22,38,40,46]  
 [17,37,45]

+3V  
 +5V  
 +PCIE\_VDDC  
 +3V\_GPU  
 GFX\_CORE

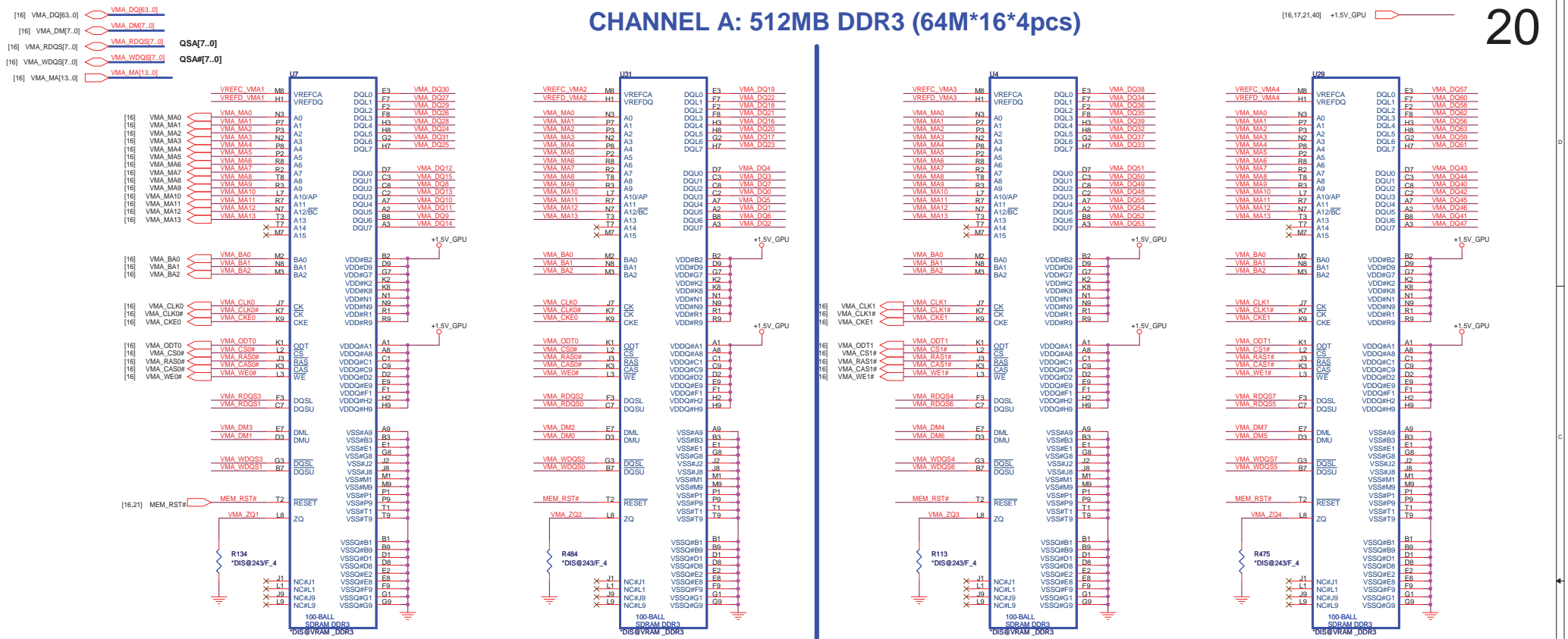


19



# CHANNEL A: 512MB DDR3 (64M\*16\*4pcs)

20

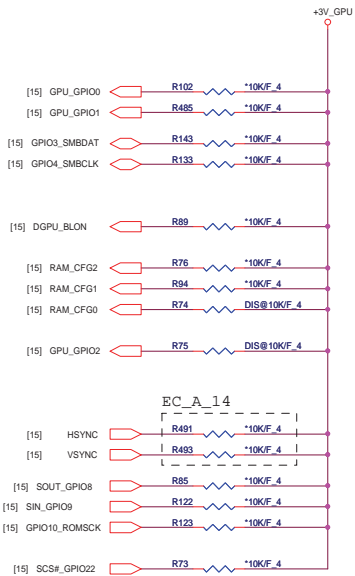


21





## PIN STRAPS



## Memory Aperture size

RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

## ROM Table

HSYNC	VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

## CONFIGURATION STRAPS

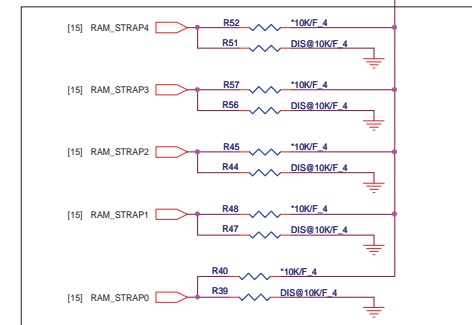
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	1	
GPIO_8_ROMSO H2SYN GPIO_21_BB_EN	GPIO8 H2SYN GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYN	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

[15,17,18,38,46] +1.8V\_GPU  
[14,15,16,17,19,38,40,46] +3V\_GPU

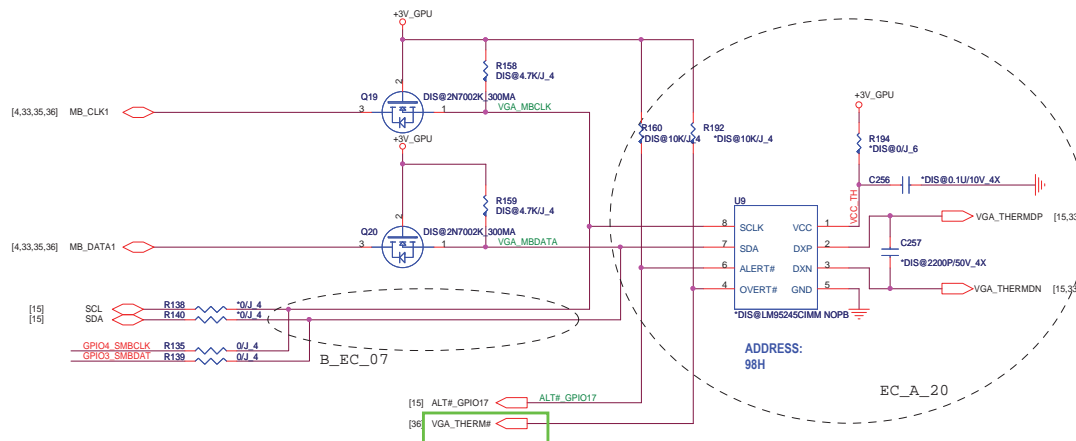
## VRAM Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4	
				15"	14"				
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW02 (64M*16-1Gb)	512MB	0	0	1	0	0	1
	H5TQ2G63BFR-11C	AKD5MGWTW00 (128M*16-1Gb)	1GB	0	0	0	0	0	1
Samsung	K4W1G1646G-BC11	AKD5EGGT500 (64M*16-1Gb)	512MB	0	0	1	1	0	1
	K4W2G1646C-HC11	AKD5MGWTW00 (128M*16-1Gb)	1GB	0	0	0	1	0	1

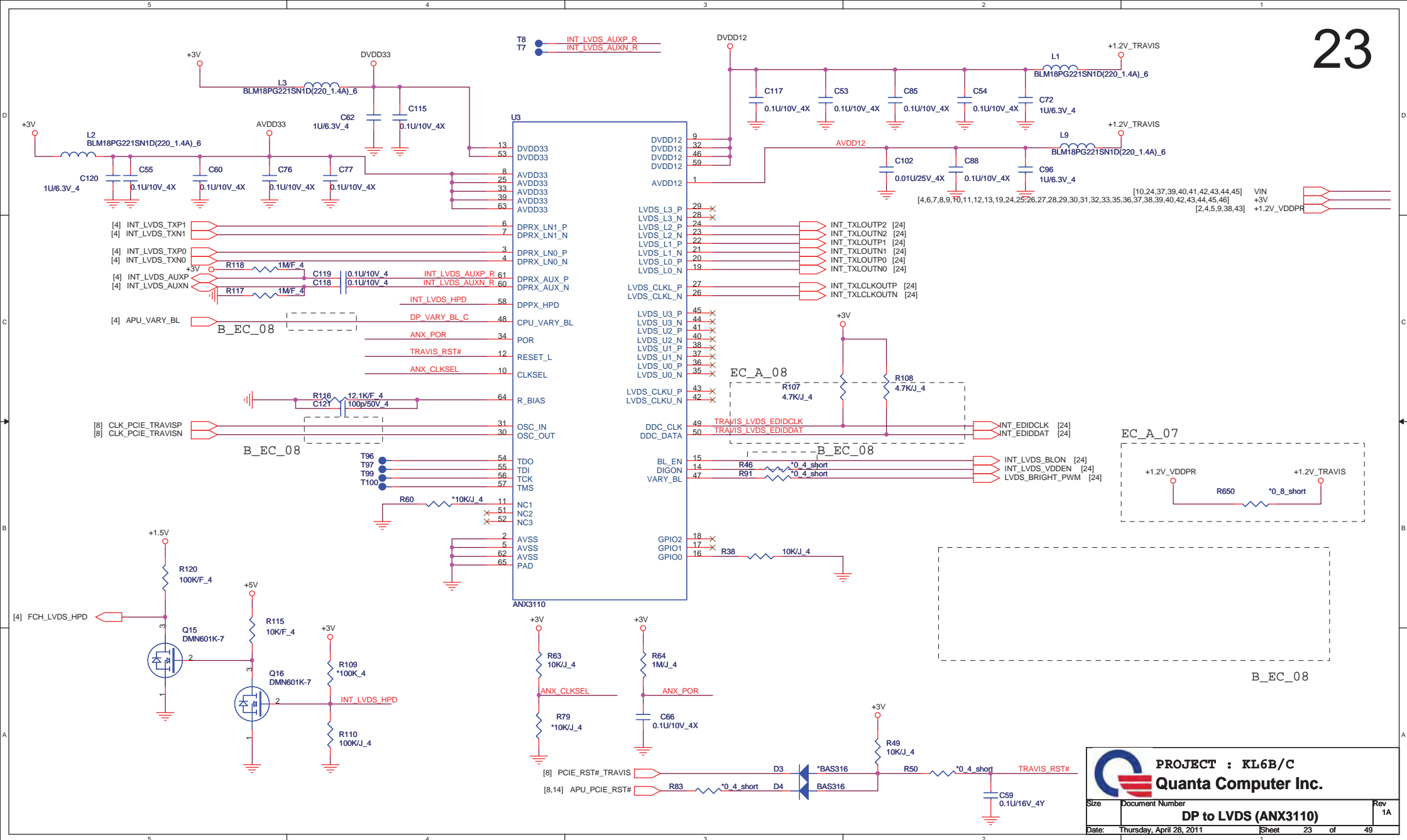
Make sure to use the correct VRAM setting

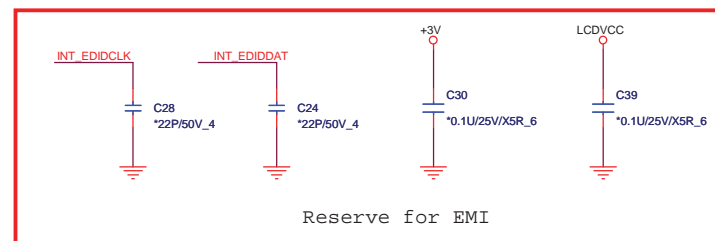
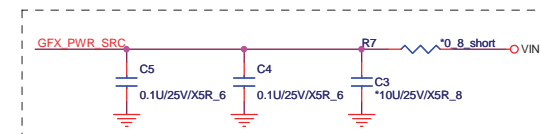


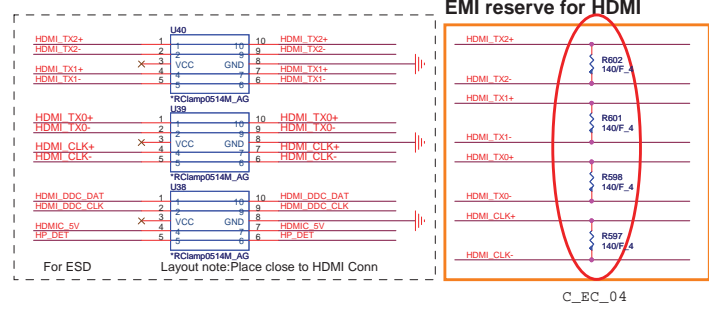
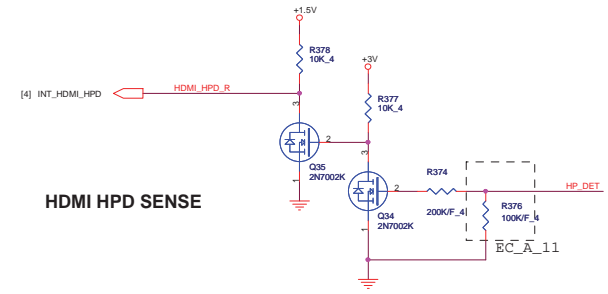
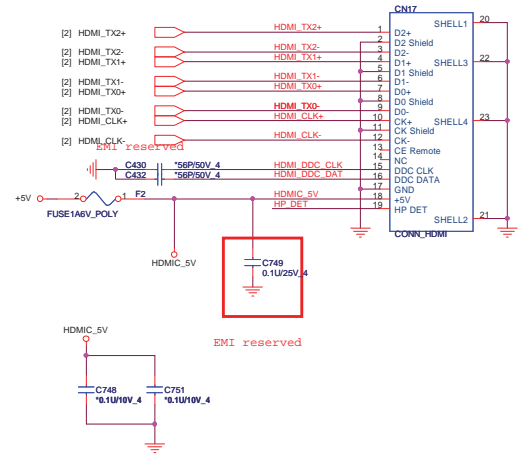
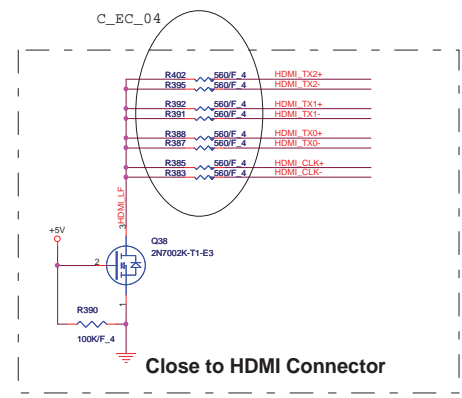
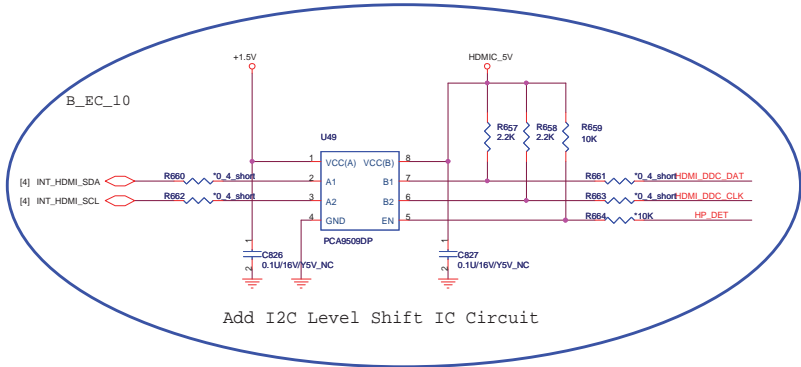
## Thermal Sensor

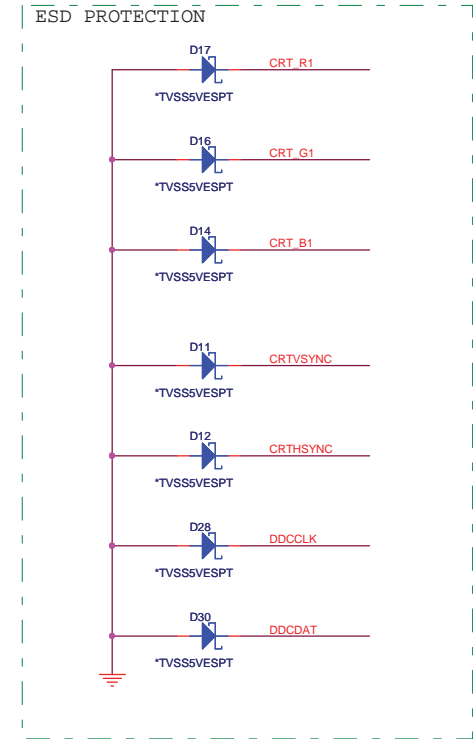
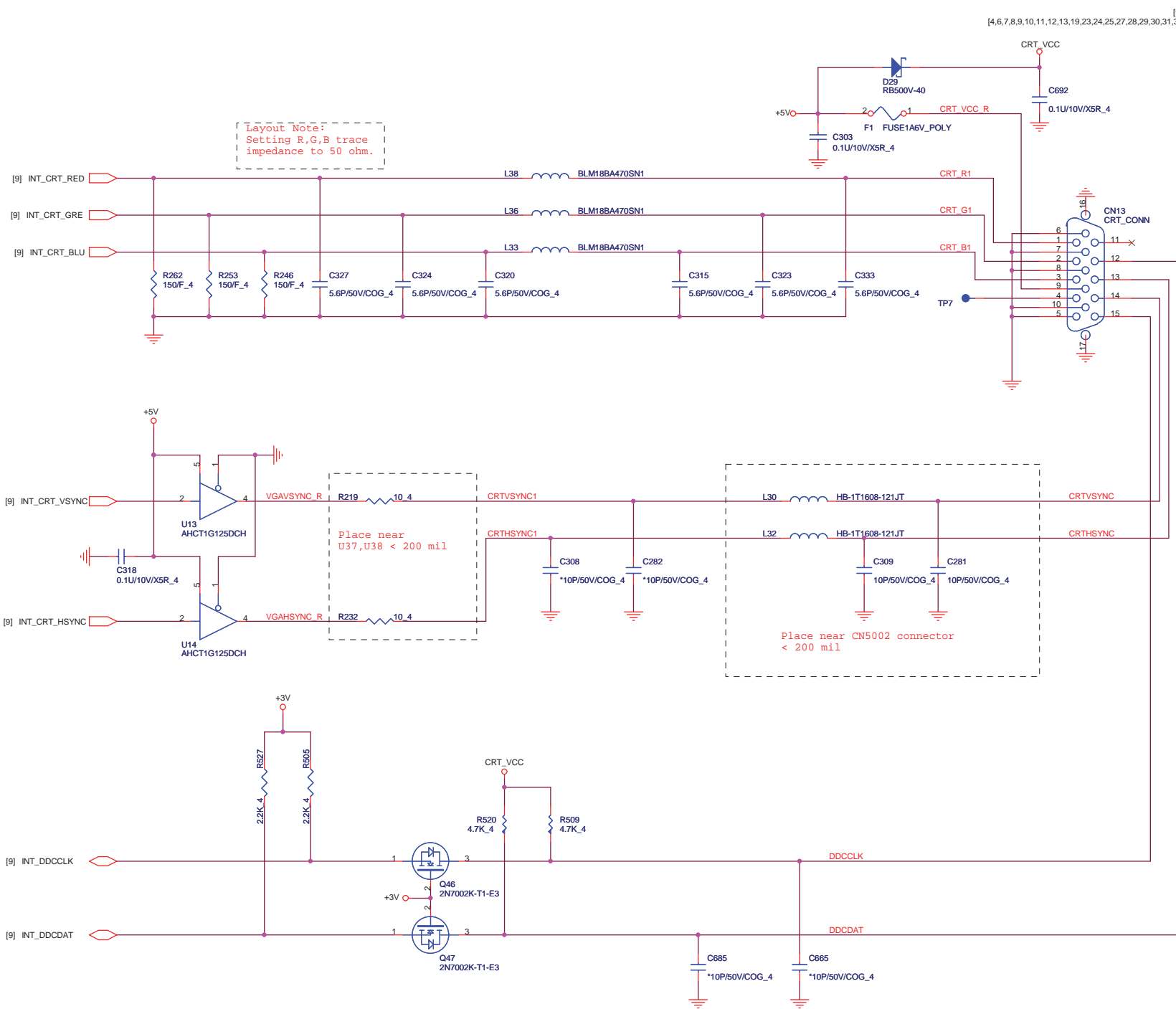










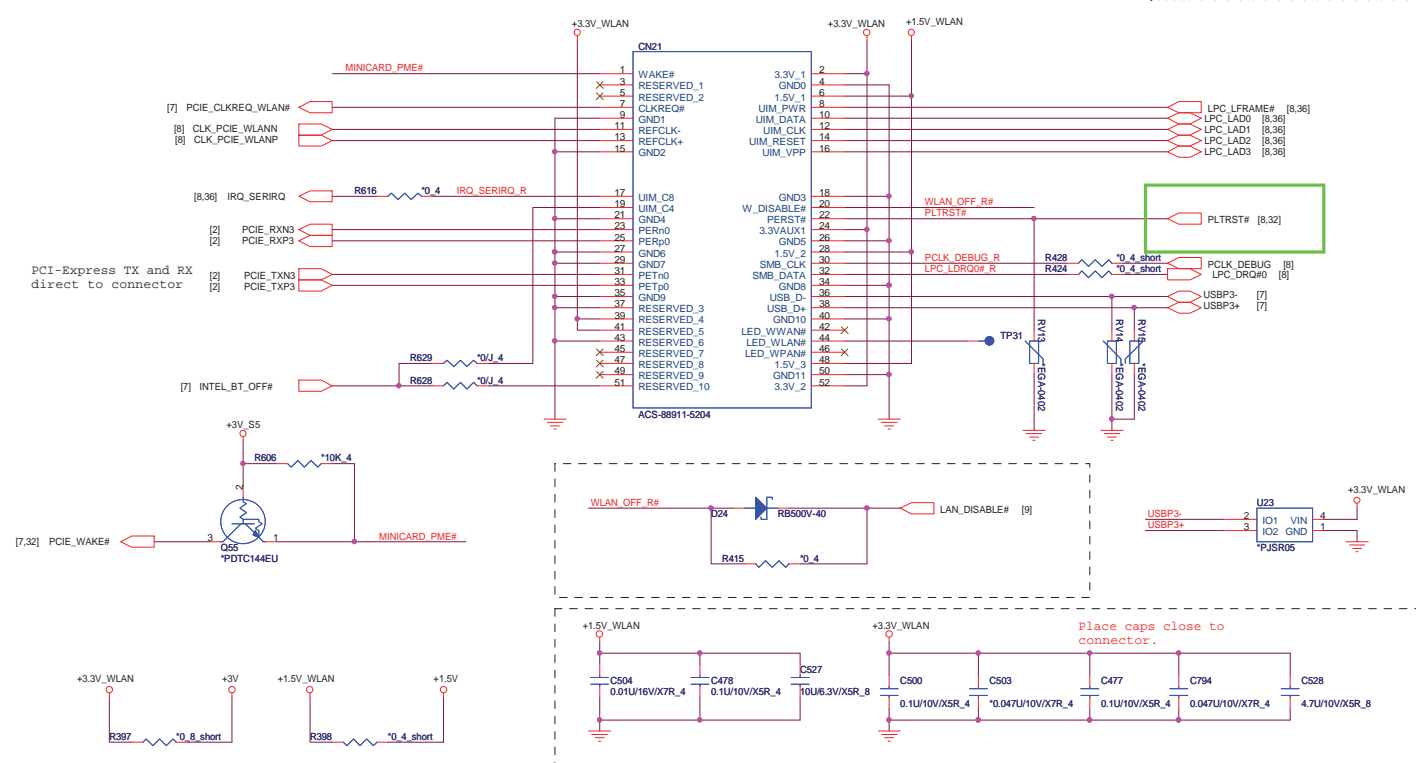
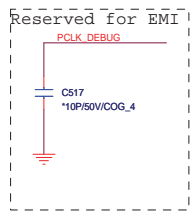


**Figure 1**

Size	Document Number
Custom	<b>Card Reader (RTS5</b>



# MiniCard WLAN connector

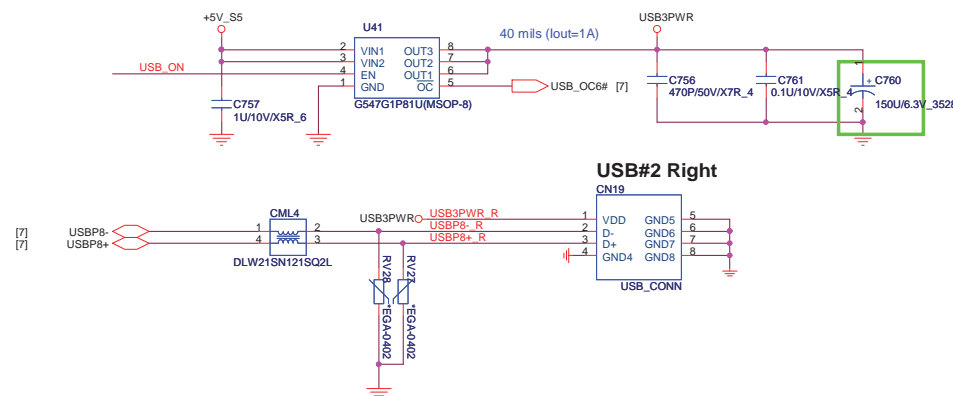
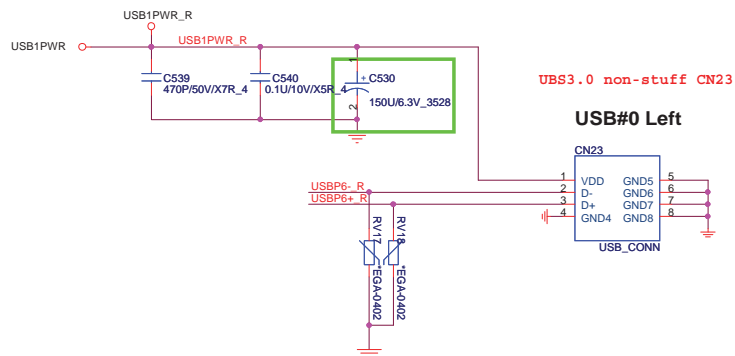
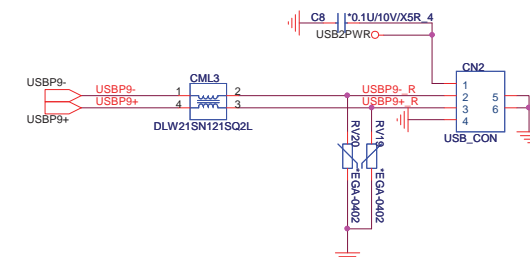
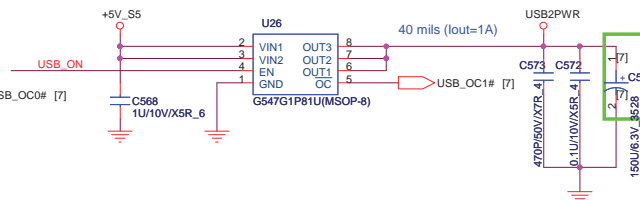




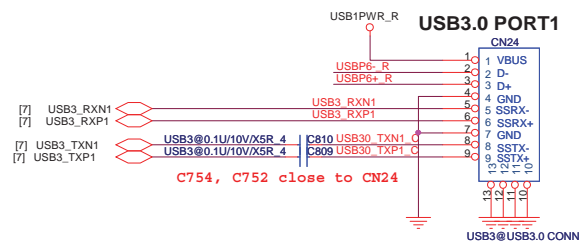




### USB#1 Daughter board

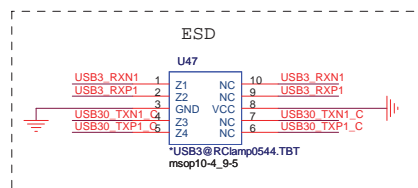
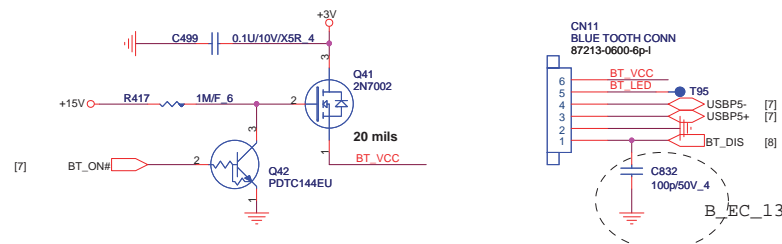


### USB3.0 PORT1

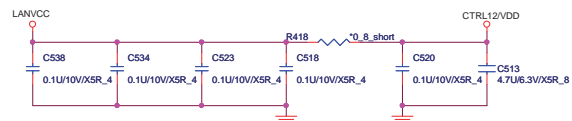
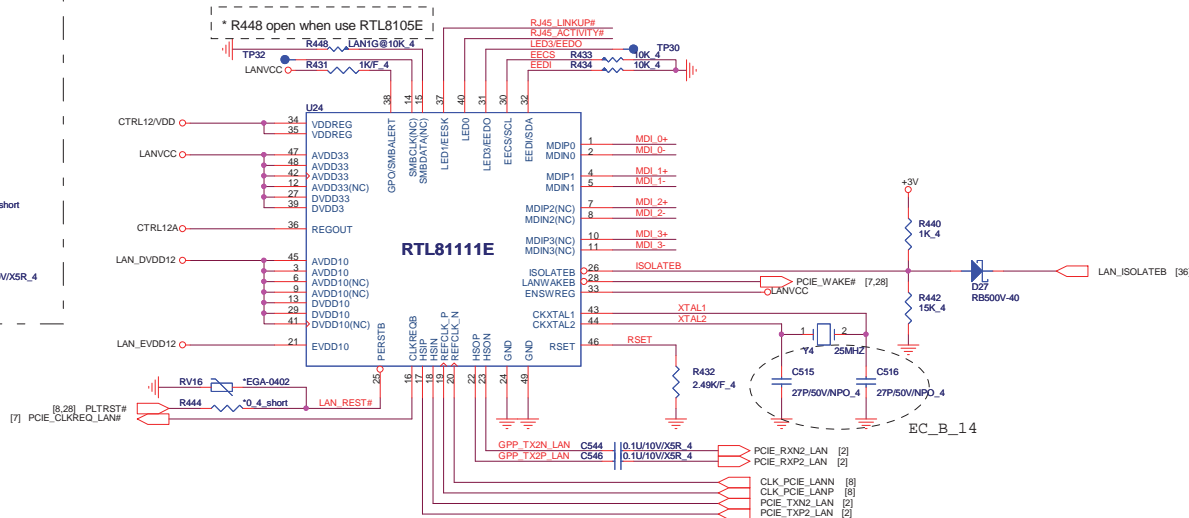
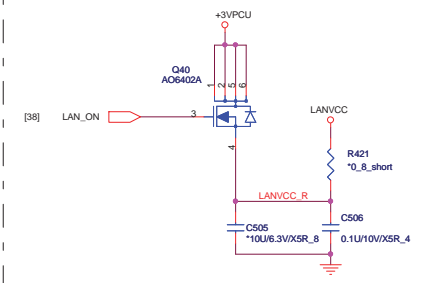


SUY USB3.0: DFHS09FR063

## BLUETOOTH

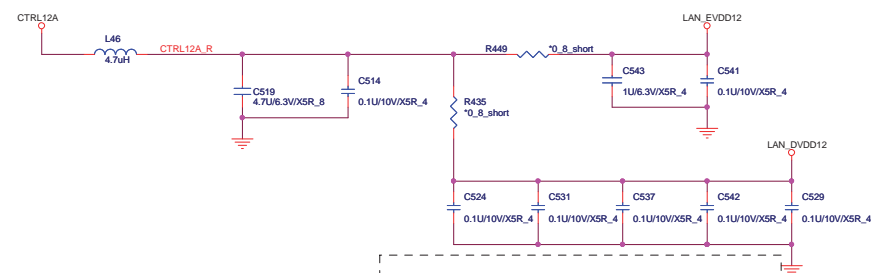


## LANVCC



\* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40.

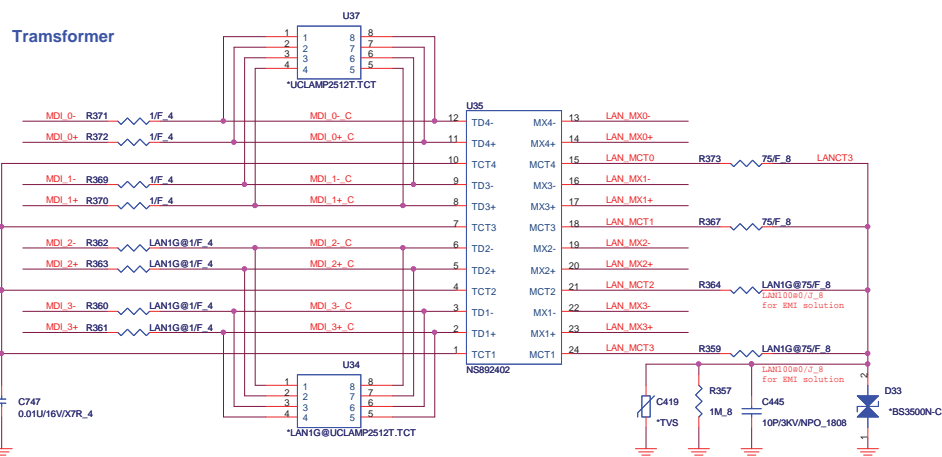
Place C5113, C5094 closed to U5006 pins 44, 45, 1 and 40.



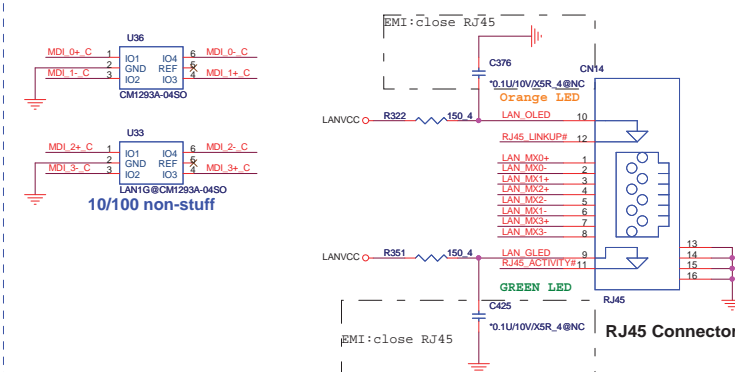
\* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

Layout: All termination signal should have 20 mil trace

## Transformer



## RJ45 Connector



PROJECT : KL6B/C  
Quanta Computer Inc.

Size Custom  
Document Number  
RTL8111EL-VB  
Date: Thursday, April 26, 2011  
Sheet 32 of 49  
Rev 1A

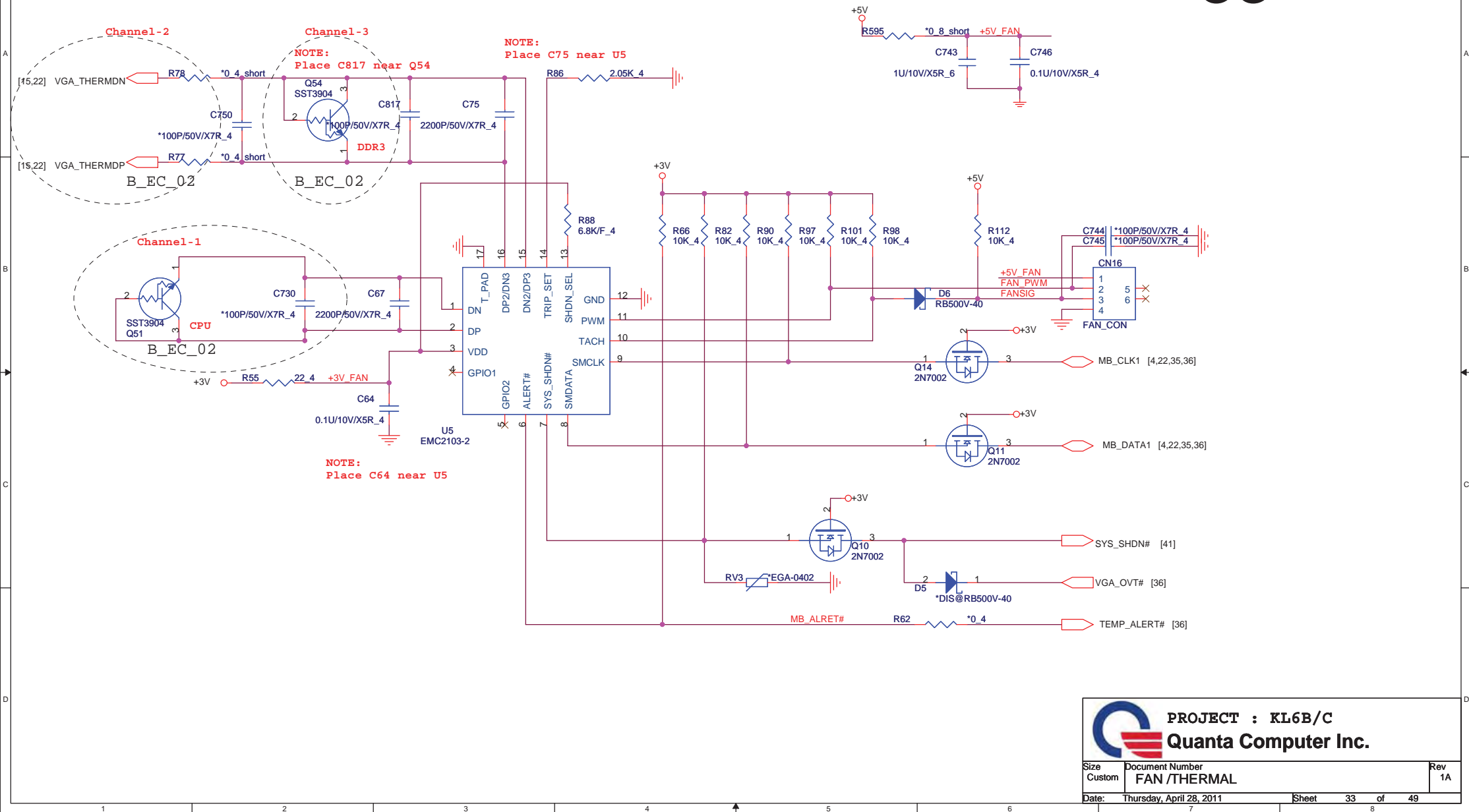
# FAN CONTROL

[4,6,7,8,9,10,11,12,13,19,23,24,25,26,27,28,29,30,31,32,35,36,37,38,39,40,42,43,44,45,46]  
[9,19,23,25,26,29,30,34,35,36,37,38,39,44]

+3V  
+5V



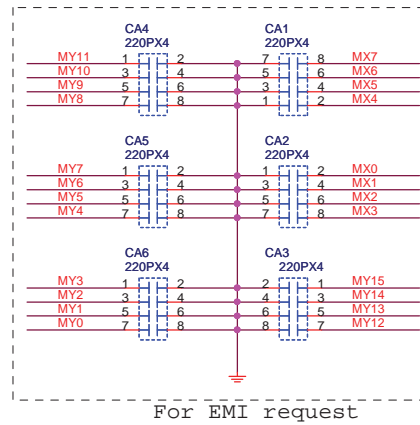
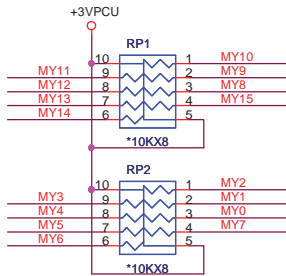
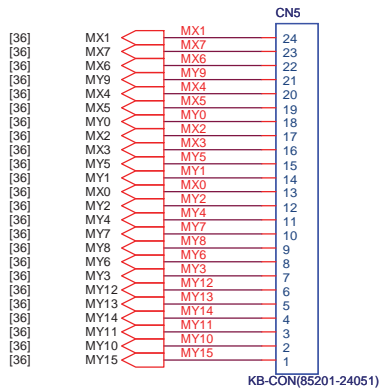
# 33



**PROJECT : KL6B/C**  
**Quanta Computer Inc.**

Size Custom	Document Number FAN /THERMAL	Rev 1A
Date: Thursday, April 28, 2011	Sheet 33 of 49	

KEYBOARD

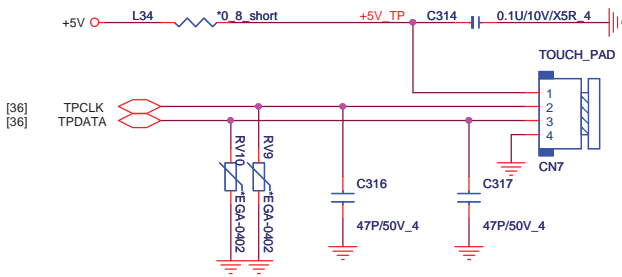


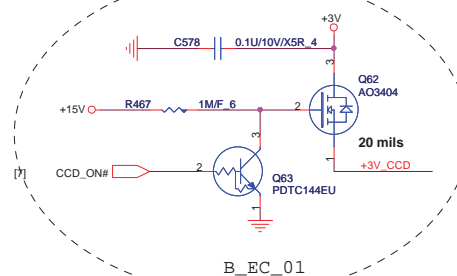
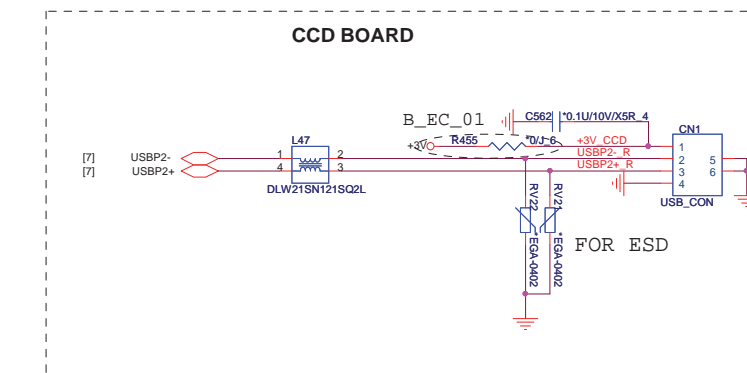
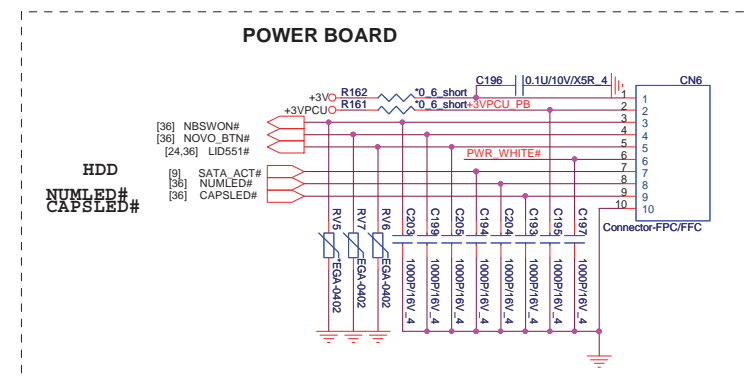
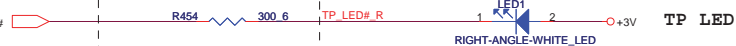
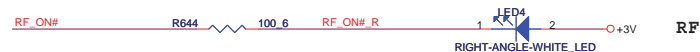
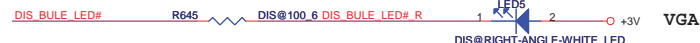
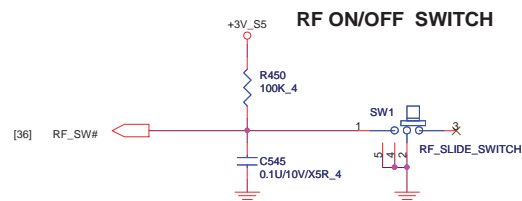
[9,19,23,25,26,29,30,33,35,36,37,38,39,44]  
[4,8,10,24,29,32,35,36,38,39,40,41,43,46]

+5V  
+3VPCU



Touch pad







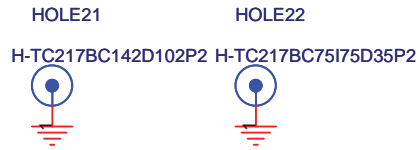


Screw for ME

CPU BKT

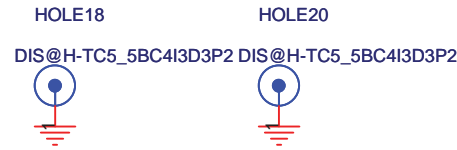
37

WLAN

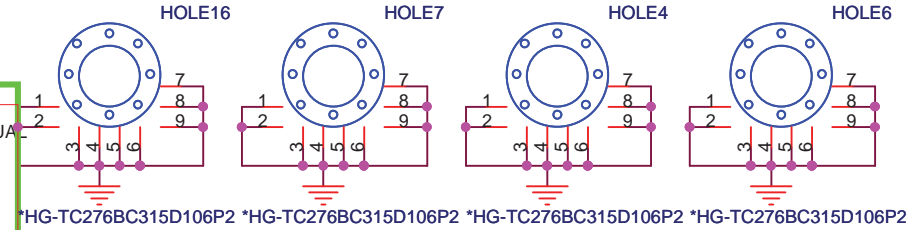
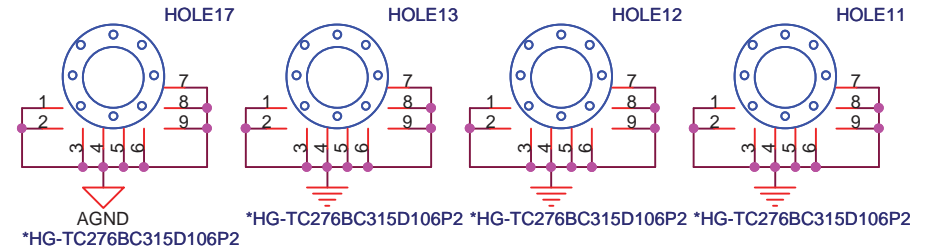
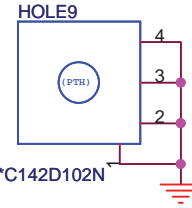


SMT NUT H=4 / 7mm

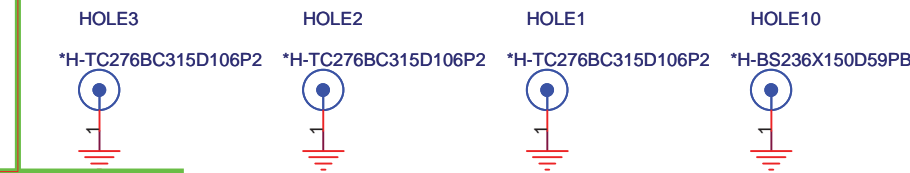
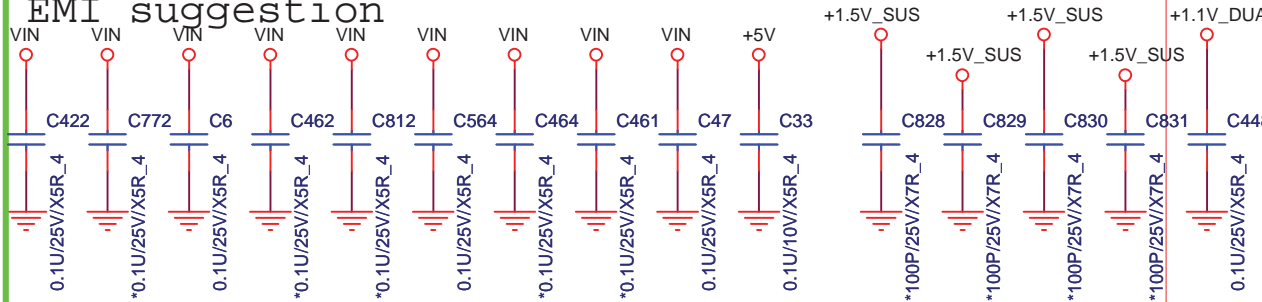
VGA



SMT NUT H=4 / 7mm



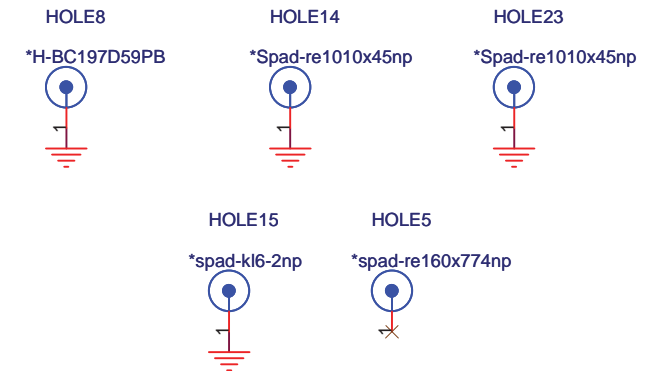
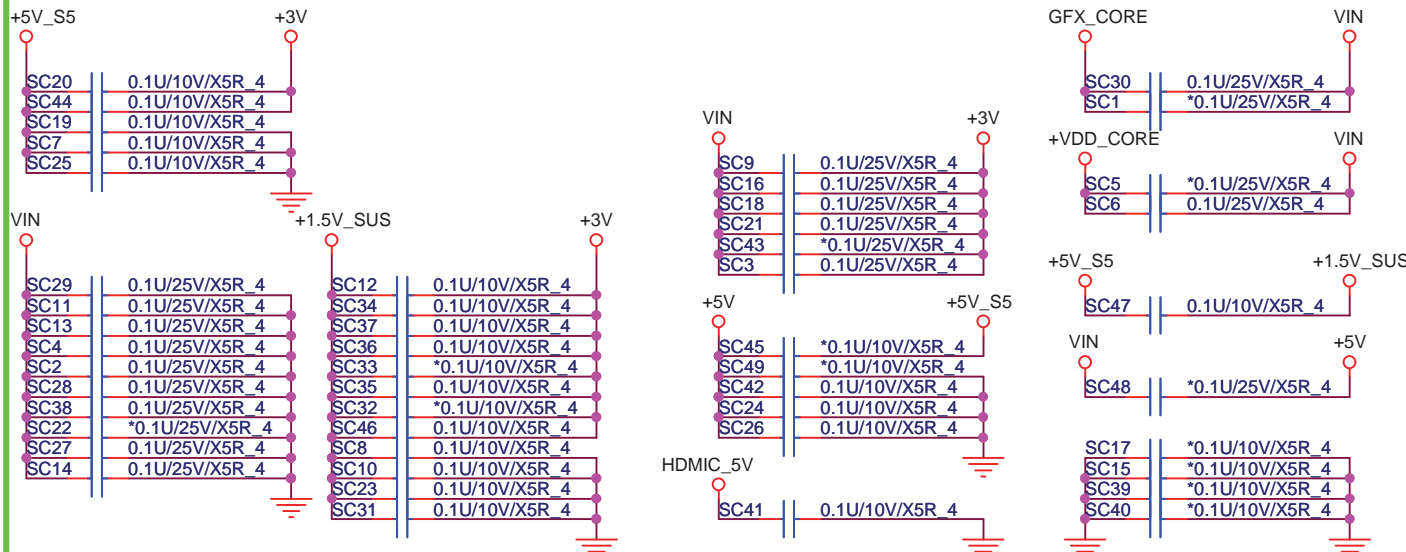
EMI suggestion



B-08

4/22 change

ESD suggestion



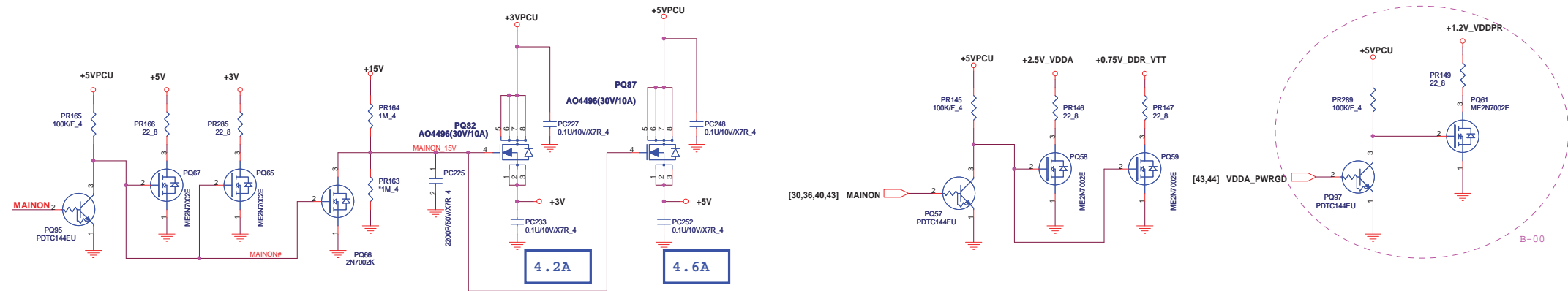
**PROJECT : KL6B/C**  
**Quanta Computer Inc.**

Size Custom Document Number **HOLD & SKEW** Rev 1A

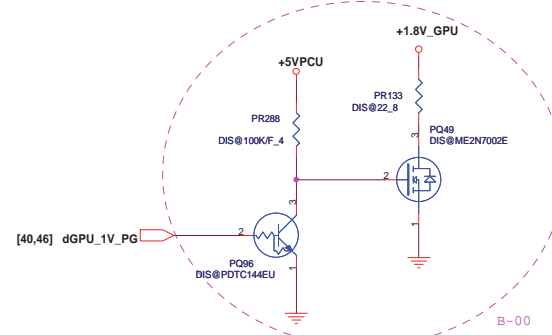
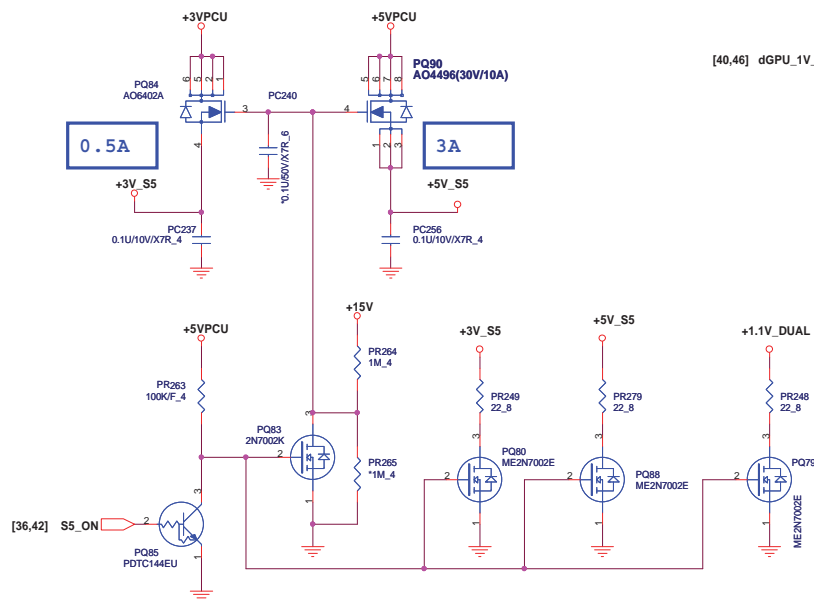
Date: Thursday, April 28, 2011 Sheet 37 of 49

## DISCHARGE

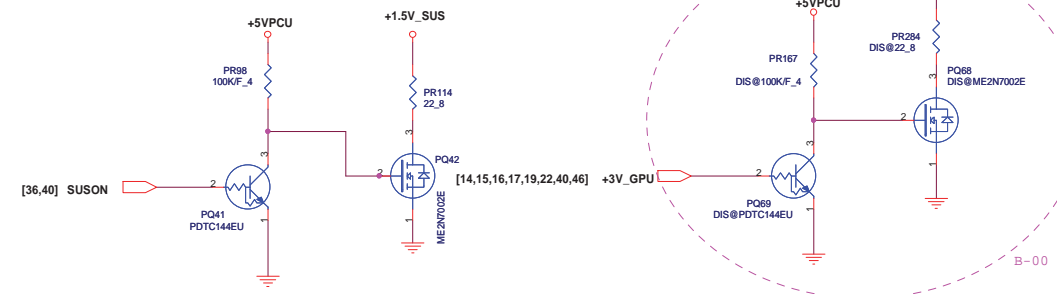
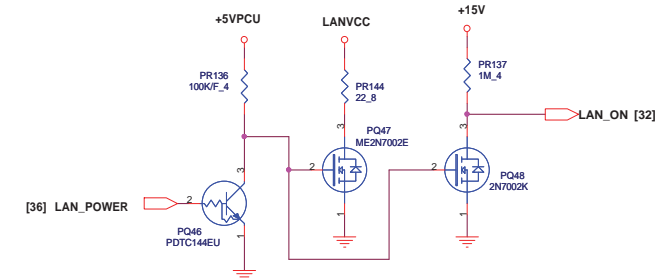
+3V, +5V, +1.5V

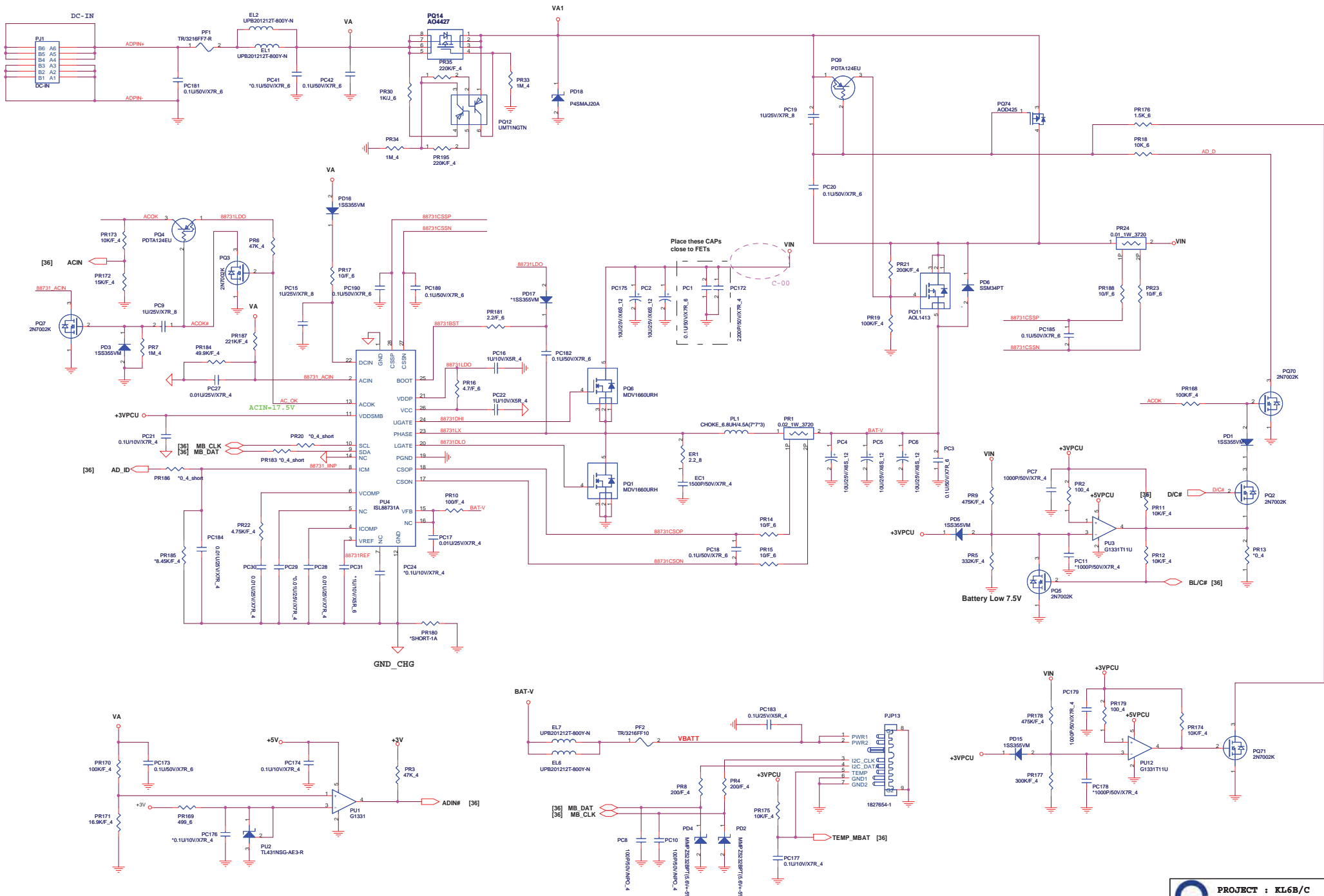


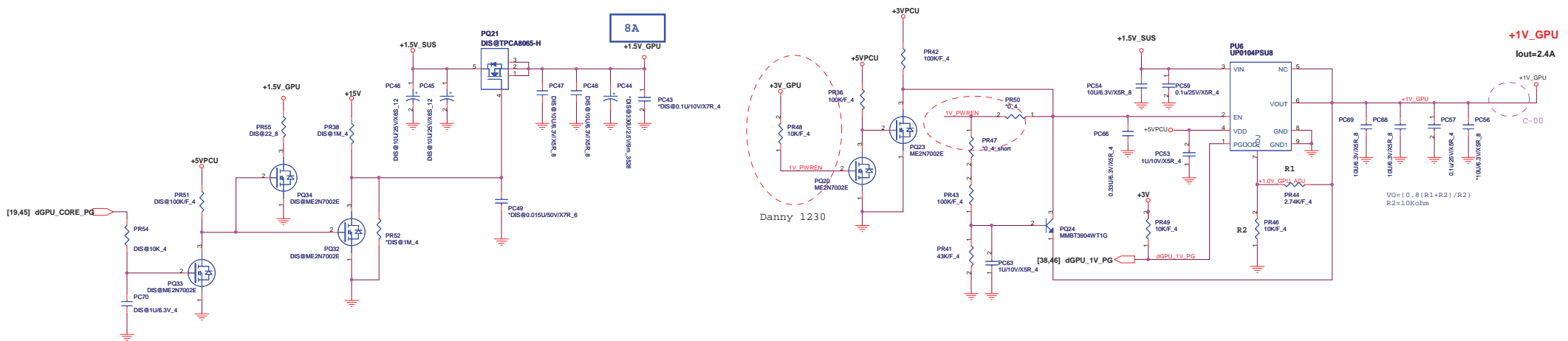
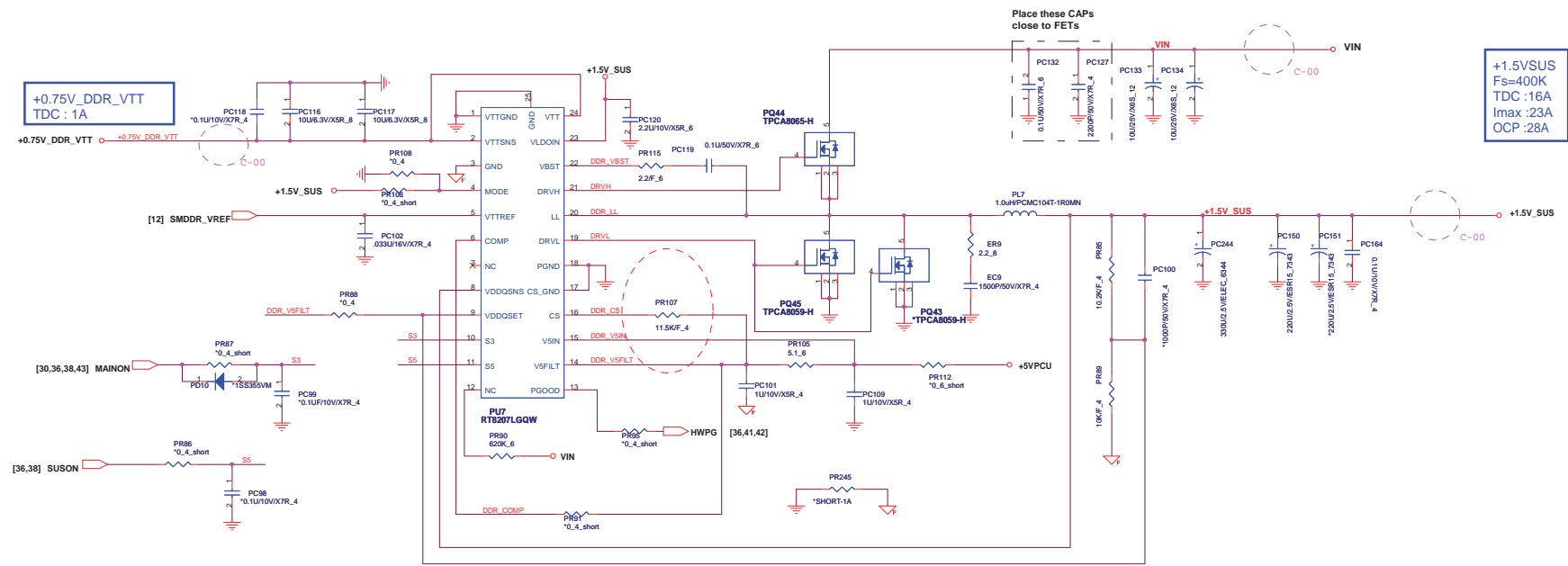
3V\_S5, 5V\_S5



## LANVCC





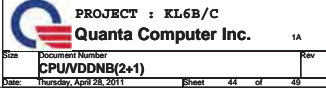


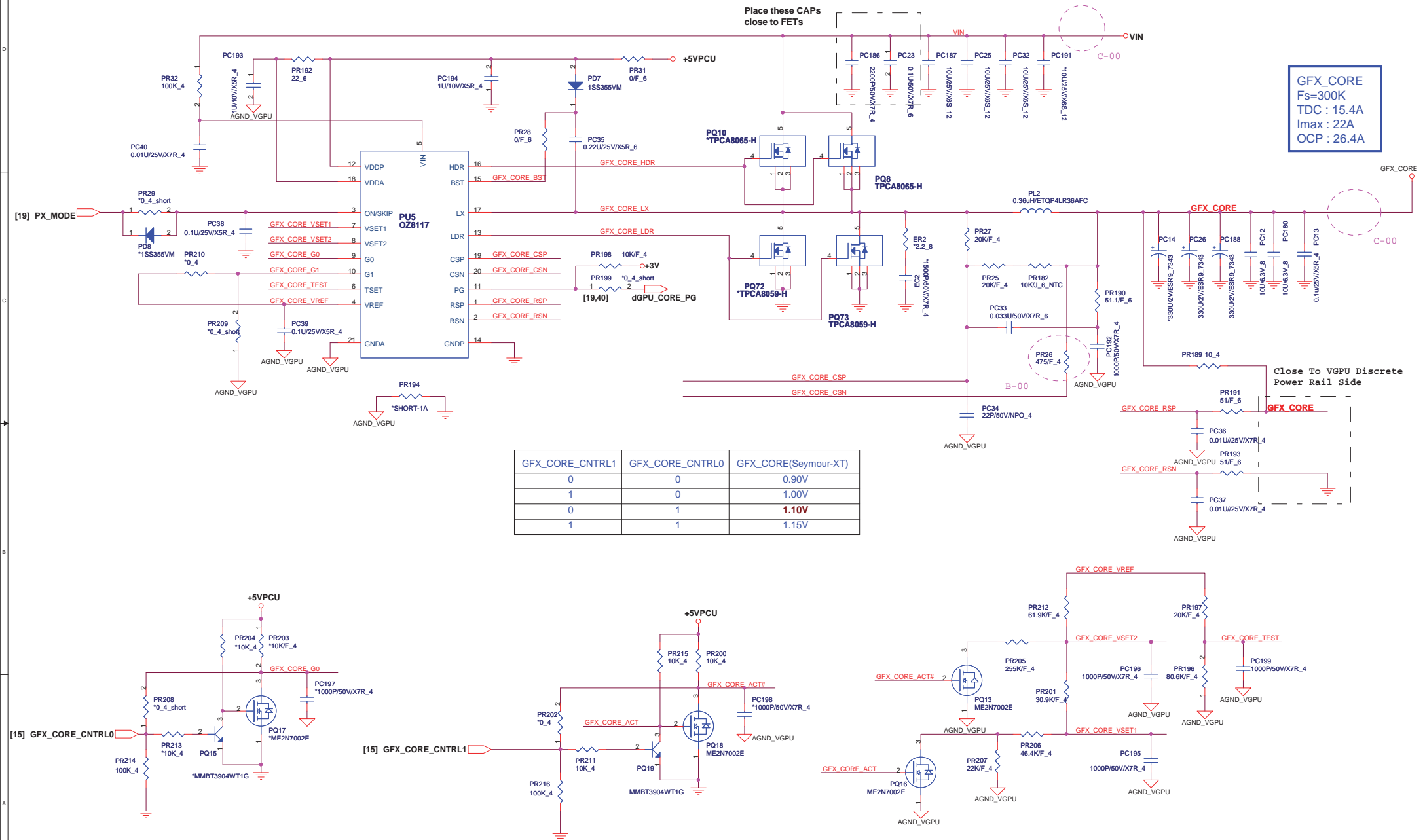


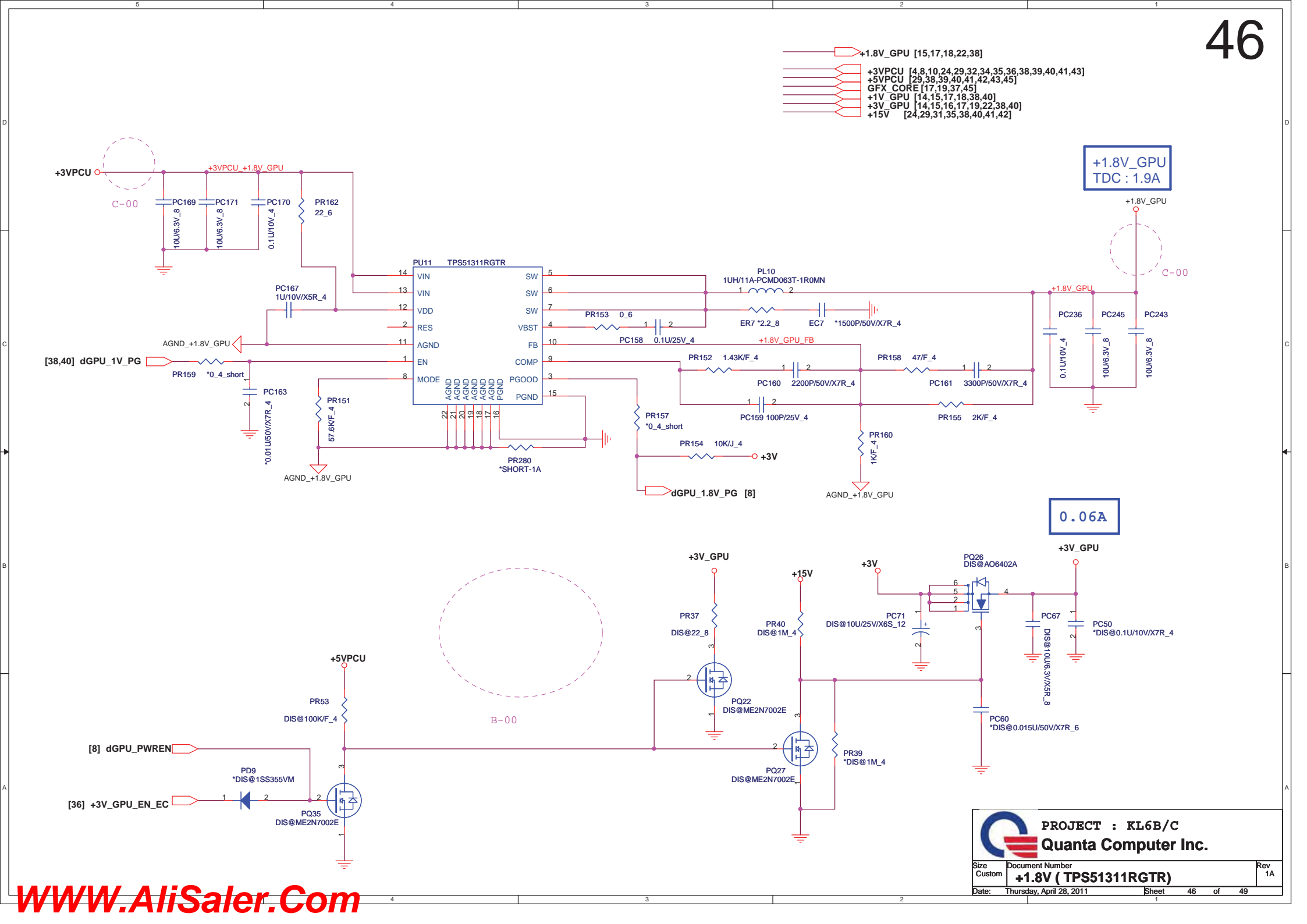




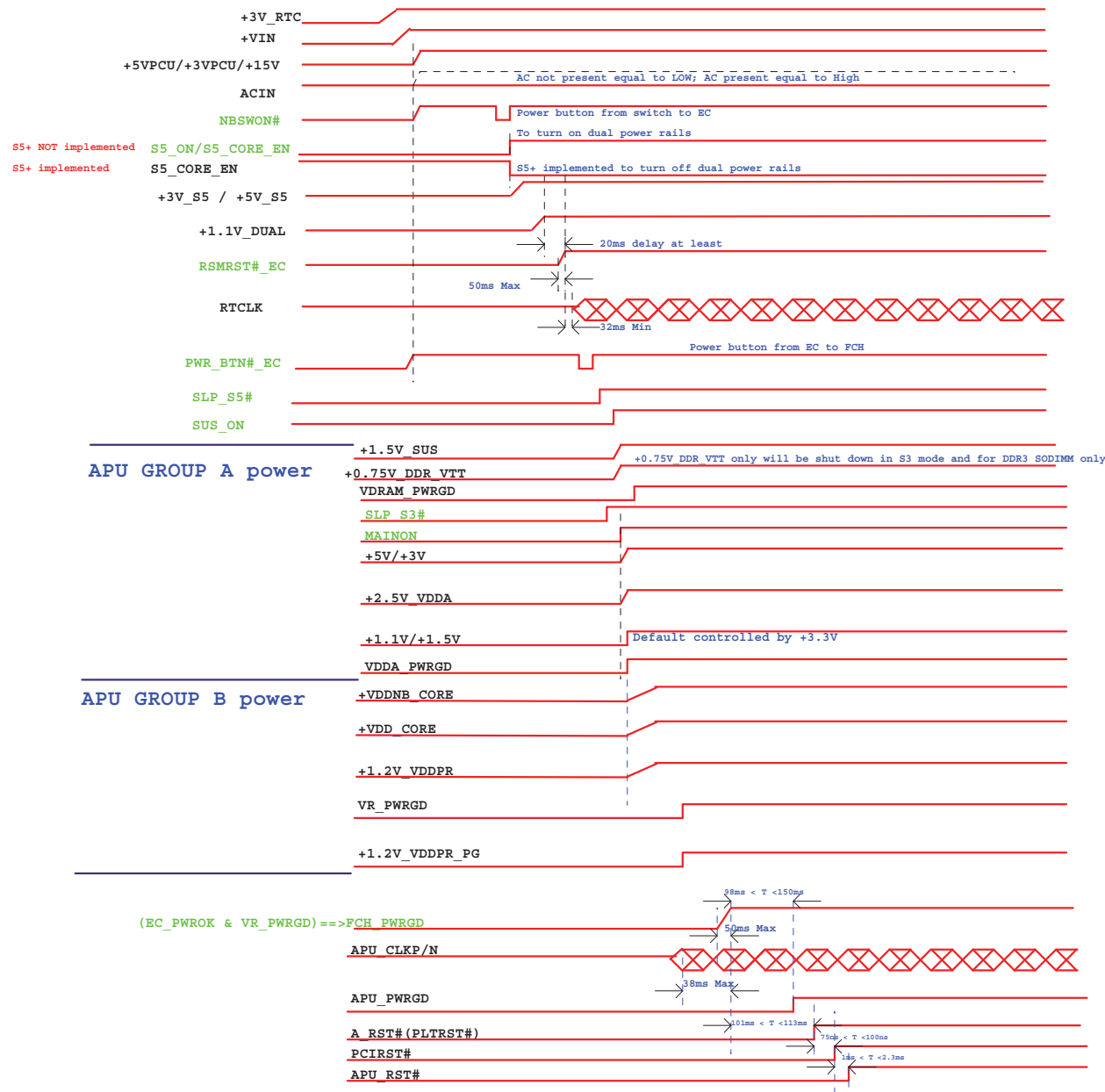








## Z475 Power On Sequence: S5 &gt; S0



## APU Power on sequence required:

Llano APU:

1.Group A ( +1.5V\_SUS, +2.5V\_VDDA ) ramp before Group B  
( +VDD\_CORE, +VDDNB\_CORE, +1.2V\_VDDPR )

HUDSON-M2/M3:

1.+3V\_S5 ramp before +1.1V\_DUAL

2.+3V ramp before +1.1V

3.+3V\_RTC must ramp at least 5 secs before the +3V\_S5

## Robson-Pro M2/Capilano-LP M2 package Power-on sequence

All power rails reach nominal within 20ms

1=&gt; +3V\_GPU

2=&gt; +VGPU\_CORE/+1V\_GPU

3=&gt; +VGPU\_CORE PWRGD to enable +1.5V\_GPU

4=&gt; +1V\_GPU PWRGD to enable +1.8V\_GPU

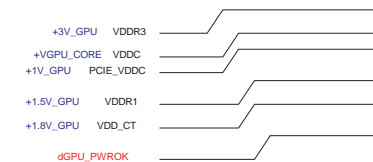
## NOTE

1.EC ( EC\_PWR\_EN ) or FCH ( PE\_GPIO1 ) to turn on +3V\_GPU

2.+3V\_GPU ready to enable +VGPU\_CORE/+1V\_GPU  
( +1V\_GPU will ramp up before +VGPU\_CORE )

3.+VGPU\_CORE PWRGD to enable +1.5V\_GPU

3.+1V\_GPU PWRGD to enable +1.8V\_GPU



## TRAVIS\_L ANX3110 power sequence

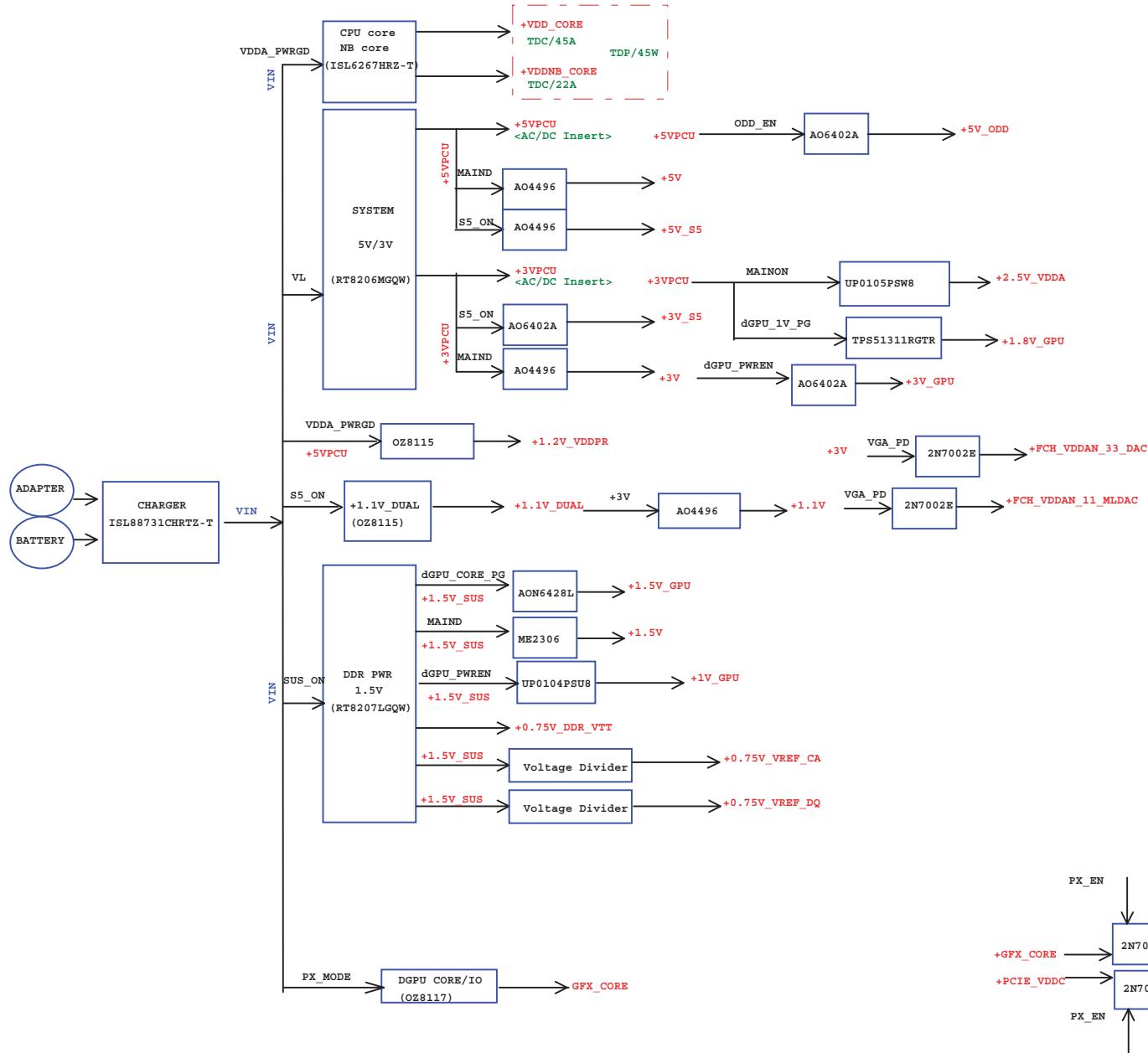
1.+3V must lead +1.2V\_TRAVIS

NOTE: EC output TRAVIS\_EN# after receive

+1.2V\_VDDPR\_PG

2.+1.2V\_TRAVIS must lead TRAVIS\_RST#

NOTE: FCH must output PCIE\_RST# TRAVIS or  
APU\_PCIE\_RST# after +1.2V\_TRAVIS ready



## KL6C / Z475 Schematic EE EC Tracking list

EC #	Page	CMVC #	Description	Date	Part Affected
A-01	4		Add level shifter design for LVDS PWM signal	0208	
A-02	4		Sys_pwrok pull high from 10K to 100K	0208	
A-03	9		Design issue need to swap SPI SI/SO signal	0208	
A-04	11		Disable Strap pin (EC disable) for CRT no function issue	0208	
A-05	14		DGPU reset change design to be controlled by GPIO only	0208	
A-06	16		Disable DGPU JTAG DEBUG MODE	0208	
A-07	23		Remove Travis IC power switch schematic for cost down	0208	
A-08	23		Desgin issue need to swap LVDS EDID signal	0208	
A-09	35		Change Resistor vaule to adjust the brighness of LED	0208	
A-10	7		Change USB port for USB2.0 & CardReader to USB.(Disable Hub3)	0208	
A-11	25		Change PU resistor value from 100ohm to 100kohm	0208	
A-12	36		Change EC pin to default PL to aviod PWR LED light one time as DC-IN	0208	
A-13	25		I2C level shift IC change to stuff.	0211	
A-14	22		no need to enable HDMI audio function in DGPU	0216	
A-15	7		Add Thermal trip PU resistor	0216	
A-16	18		Remove bead & cap for cost down	0218	
A-17	35		Add R188 ODD_MDDA# to connect to EC	0224	
A-18	35		Remove VGA SW2(ATI can't support HW switchch)	0224	
A-19	22		Remove VGA External thermal IC	0224	
SIV					
B-01	35		Add CCD P_SW on/off (Add C578, Q62, R467, Q63, R468 ; Del R455)	0306	
B-02	33		Connect to VGA Therm_Die use Channel 1.Del Q58(WLAN) to for CPU used. Add: R78, R77 ; Del: Q58	0306	
B-03	9		Change U17 VDD to +3V_S5	0306	
B-04	9		ADD SPI_HOLD# GPIO control, reserve R469	0306	
B-05	4		ADD SM_LV_CLK & SM_LV_DAT to connect FCH; Reserve R496 & R497	0306	
B-06	9		AUXCAL change to power rail for VGA Power Down Feature	0306	
B-07	22		ADD MOSFET for VGA SMBUS; ADD Q19, Q20, R158, R159	0306	
B-08	23		Del R8 ,R177,R99, R41,R42,R43 for remove LVDS reserve schematic	0307	
B-09	25		Delete R389,R401,D20,D21,D22,D23,Q36,Q37 cost reduce fail	0316	
B-10	25		Add R657,R658,R659,R660,R661,R662,R663,R664,C826,C827,U49	0316	
			2nd source verify	0316	
B-11			EMI solution	0316	
			POP R602,R601,R598,R597 120ohm	0316	
			POP CML3,CML4,CML2,CML1,L47	0316	
			Remove R464,R456,R599,R600,R451,R453,R412,R413,R465,R466 0ohm	0316	
			POP C408,C422,C749	0316	
			POP C391,C392	0316	
			Reserve C828,C829,C830,C831	0316	
B-12	06		POP R655,R656 Remove U18,R337,R330 Internal notice update	0317	
			Change Q61 PN:BA05L060000 Internal notice update	0317	
			Remove C207	0317	
B-13	34		CN5 Modify footprint to 85208-24071-24p-1	0317	
B-13	31		Add C832 for EMI solution	0318	
B-14			Change C515 & C516 to 27pF to fine tune timing	0321	
			Change C387 & C386 to 27pF to fine tune timing	0321	
			Change C188 & C184 to 27pF to fine tune timing	0321	
			Change C365 & C366 to 27pF to fine tune timing	0321	
SVT					
C-01	04		Change R541,R547 to *0_4_short	0418	
	06		Change R535,R537,R545 to *0_4_short	0418	
			Delete U18,R655,R656,R337,R330; J1,R587,R336,R323,R305,R580,R577	0418	
	07		Change R468,R287,R545,R169, R521,R533,R256,R317,R258,R552,R528 to *0_4_short	0418	
	08		Change R200,R183 to *0_4_short; Change R427 to *0_6_short	0418	



Document Number  
**EC Tree**

Document Number  
**EC Tracking Record A**

Rev	1A
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EC #	Page	CMVC #	Description	Date	Part Affected
C-01	09		Change R263,R254,R247 to *0_4_short	0418	
	19		Change R157 to *0_4_short	0418	
	23		Change R83,R50,R46,R91 to *0_4_short; change R650 to *0_8_short	0418	
	24		Change R2 to *0_4_short; Change R7,R28 to *0_8_short	0418	
	25		Change R660,R661,R662,R663 to *0_4_short	0418	
			Delete U42,R603,R605, R381,R382,R384,R386,R399,R400; C375, C377,C448,C449,C459	0418	
	28		Change R398,R424,R428 to *0_4_short	0418	
			Change R397 to *0_8_short	0418	
	29		Change CML1 footprint to "choke-wcm2012-4p"	0418	
			Delete R412,R413; Change R365,R3698,R604 to *0_8_short	0418	
	31		Change R438 to *0_4_short	0418	
			Change CML2,CML3,CML4 footprint to "choke-wcm2012-4p"	0418	
			Delete R451,R453,R599,R600,R456,R464	0418	
	32		Change R444 to *0_4_short; Change R418,R421,R435,R449 to *0_8_short	0418	
	33		Change R77,R78 to *0_4_short; Change R595 to *0_8_short	0418	
	34		Change L34 to *0_8_short	0418	
	35		Change L47 footprint to "choke-wcm2012-4p"	0418	
			Delete R465,R466; Change R161,R162 to *0_6_short	0418	
	36		Change R111,R142,R188,R203 to *0_4_short	0418	
	27		Change R646 to *0_8_short	0418	
	12		Change R394 to *0_6_short	0418	
C-02	31		change U47 Pin8 design	0422	
	37		Add C448 (0.1u CAP) for EMI solution	0422	
C-03	4		delete APU debug funciton, R570, R579,R583,R584,R596	0425	
	34		Mount CA1,CA2,CA3,CA4,CA5,CA6 for EMI solution	0426	
	35		Change Q62 PN to BAM34040001	0426	
	10		Change Q29,Q32 PN to BAM34040001	0426	
C-04	25		Change value of R601,R602,R597,R598 to 140 ohm for HDMI issue	0428	
			Change value of R383,R385,R387,R388,R391,R392,R395,R402 to 560 ohm for HDMI issue	0428	



Size Custom	Document Number <b>EC Tracking Record B</b>	Rev 1A
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